

the number of receivers or packet drops in the network. Our protocol exhibits two features: it avoids the undesirable feedback implosion phenomenon and it uses minimum total bandwidth.

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Bismuth nano-Hall probes fabricated by focused ion beam milling for direct magnetic imaging by room temperature scanning Hall probe microscopy

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Bismuth nano-Hall probes with dimensions $\sim 120 \times 120$ nm were fabricated by focused ion beam milling and used for the direct room temperature magnetic imaging of crystalline garnet thin films and strontium ferrite permanent magnets by scanning Hall probe microscopy. At driving currents of $40 \mu\text{A}$, the Hall coefficient and magnetic field sensitivity of the Bi nano-Hall probes were $3.3 \times 10^{-4} \Omega/\text{G}$ and $7.2 \text{ G}/\sqrt{\text{Hz}}$, respectively.

Introduction: Scanning Hall probe microscopy is a promising method for the non-invasive and direct imaging of magnetic domains [1–3]. We have previously reported on the use of a new room temperature scanning Hall probe microscope system (RT-SHPM) incorporating a GaAs/AlGaAs heterostructure micro-Hall probe (HP) for directly imaging ferromagnetic domains [4]. In spite of excellent results obtained using this system, the use of semiconductor micro-Hall probes was found to be impractical at room temperature for device dimensions $< \sim 1.0 \mu\text{m}^2$ owing to surface charge depletion effects that limit the maximum Hall probe drive current to $\sim 2 \mu\text{A}$ and a large Johnson noise component due to the large series resistance of $70 \text{ k}\Omega$ [5]. More recently, we reported an alternative approach to room temperature scanning Hall probe microscopy using $2.8 \times 2.8 \mu\text{m}^2$ bismuth (Bi) Hall probes exhibiting negligible surface charge depletion effects and a lower series resistance than GaAs/AlGaAs probes [6].

To reduce the size and thereby improve spatial resolution of the Bi micro-Hall probes, we describe in this Letter the fabrication of $\sim 120 \times 120$ nm Bi nano-Hall probes (nano-HP) by focused ion beam (FIB) milling and their use for the direct magnetic imaging of ferromagnetic domains by RT-SHPM. FIB was found to be a direct and reproducible means of fabricating nanometre-sized Bi Hall probes.

Experiment: The Bi nano-HPs were fabricated on 5×5 mm, semi-insulating (100) GaAs substrates. The initial processing involved the use of photolithography to define Bi micro-Hall probes as follows: (i) evaporation of a 70 nm-thick Bi Hall bar element onto the GaAs substrate through a patterned photoresist window from a thermally-heated boat source in a vacuum of 1×10^{-6} Torr, at a rate of 1 nm/s ; (ii) lift-off in acetone to define $\sim 2.8 \times 2.8 \mu\text{m}$ Bi micro-Hall probe structure $\sim 13 \mu\text{m}$ away from the corner of the chip; (iii) photolithography and lift-off to define $400 \times 400 \mu\text{m}$ bond pads (30 nm Cr/150 nm Au); (iv) patterning to define STM-

tip pad, consisting of a window overlapping a $1 \mu\text{m}$ deep mesa at the chip corner; (v) deposition of STM-tip metals (15 nm Cr/20 nm Au) by thermal evaporation at 1×10^{-6} Torr. The resulting Bi micro-Hall probe was then bonded onto packages using $12 \mu\text{m}$ Au wires.

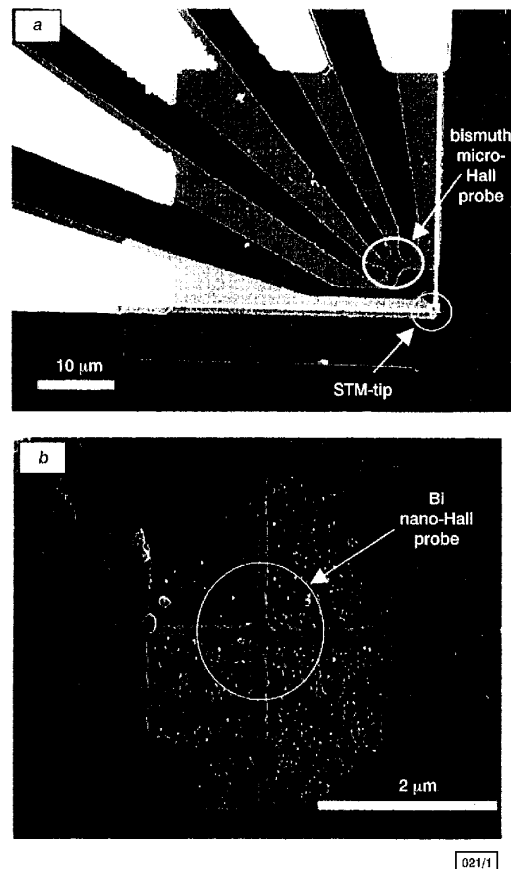


Fig. 1 SEM images of Bi micro-Hall and Bi nano-Hall probes

a Bismuth micro-Hall probe fabricated using optical lithography
b Bismuth nano-Hall probe fabricated by focused ion beam milling of Bi micro-Hall probe

The dimensions of the active 'cross regions' of the resulting Bi micro-Hall probes were reduced to the nanometre scale by FIB milling using a Hitachi FB-2000A FIB system. Typical FIB milling conditions employed ion currents and voltages of $15 \text{ A}/\text{cm}^2$ and 30 kV , respectively. Fig. 1*a* shows a scanning electron microscope (SEM) image of a typical Bi micro-Hall probe. Fig. 1*b* is a typical SEM image of a $\sim 120 \times 120$ nm Bi nano-HP produced by FIB milling of the Bi micro-Hall probe. When present, the slight remnants of the Bi film as seen in Fig. 1*b* did not have any detrimental effects on device performance.

The Bi nano-Hall probes were mounted onto the piezoelectric scanning tube of the RT-SHPM at a tilt angle of 1.5° and scanned over the sample surface while recording changes in Hall voltage due to fluctuations of the stray magnetic flux normal from the surface. A detailed explanation of the measurement procedure is provided in [4]. The tunnel current of an STM-tip fabricated adjacent to the Hall probe was simultaneously monitored for topographic imaging of the sample surface. The black and white regions of RT-SHPM scan images represent magnetic domains with magnetisations into and out of the plane of the paper.

Results and discussion: The Hall coefficient and series resistance of the $\sim 120 \times 120$ nm Bi nano-HP were $3.3 \times 10^{-4} \Omega/\text{G}$ and $5.2 \text{ k}\Omega$, respectively. The Johnson noise was measured to be $110 \text{ nV}/\sqrt{\text{Hz}}$ at a driving Hall current of $40 \mu\text{A}$ with the resulting field sensitivity being $7.2 \text{ G}/\sqrt{\text{Hz}}$.

All the RT-SHPM images described below were measured by simultaneously monitoring both the STM-tip tunnel current and Bi nano-Hall probe signal. Under such measurement conditions, the Bi nano-Hall probe was $0.27 \mu\text{m}$ above the sample surface.

Fig. 2 shows a $20 \times 20 \mu\text{m}$ RT-SHPM magnetic image of a $5.5 \mu\text{m}$ -thick crystalline bismuth substituted iron garnet thin film. The graph shows the variation of the magnetic field along the line drawn on the image. These field values are consistent with measurements carried out using GaAs/AlGaAs micro-Hall probes [4].

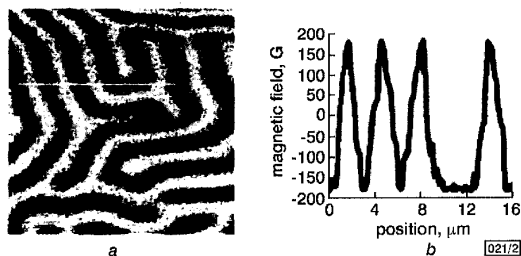


Fig. 2 RT-SHPM magnetic image of bismuth substituted iron garnet thin film and corresponding magnetic field variation

a $20 \times 20 \mu\text{m}$ RT-SHPM magnetic image of $5.5 \mu\text{m}$ -thick bismuth substituted iron garnet thin film
b Magnetic field variation along line in a

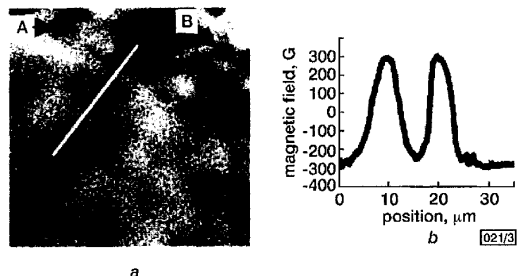


Fig. 3 RT-SHPM magnetic image of strontium ferrite permanent magnet and corresponding field variation

a $50 \times 50 \mu\text{m}$ RT-SHPM magnetic image of surface of polished strontium ferrite permanent magnet
b Corresponding field variation along line in a

Fig. 3 shows a $50 \times 50 \mu\text{m}$ RT-SHPM magnetic image of a polished $300 \mu\text{m}$ -thick demagnetised strontium ferrite permanent magnet showing ferromagnetic domains with fields varying as shown in the cross-section graph. There was no correlation between the magnetic and topographical images of the sample surface. Domains as small as those marked 'A' and 'B' were not resolved in previous experiments using $\sim 1 \mu\text{m}^2$ GaAs/AlGaAs HP [4], thus demonstrating the improved spatial resolution possible with the Bi nano-HP.

Conclusion: Bismuth nano-Hall probes were fabricated by FIB ion milling and successfully used for the direct magnetic imaging of domains structures in low coercivity garnets and demagnetised Sr ferrite permanent magnets by RT-SHPM. The Bi nano-probes overcome limitations due to surface depletion and large series resistances associated with semiconductor micro-Hall probes. We are studying ways of further improving the spatial and field resolution of the Bi nano-HPs.

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56 Gbit/s analogue PLL for clock recovery

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A clock-recovery circuit is reported that employs a phase-locked loop (PLL) at 56.88 Gbit/s, and is demonstrated by locking to a 28.44 GHz sinusoidal signal while two additional circuits with adapted on-chip passive components are locked to 29 and 39 Gbit/s pseudorandom bit sequences. To the knowledge of the authors, this is the first demonstration of an integrated PLL integrated circuit for clock recovery at a data rate well above 40 Gbit/s.

Introduction: 40 Gbit/s circuits for SONET applications are now moving from research situations towards commercial applications, being implemented both in processes of moderate speed and high device count (Si, SiGe) or high-speed processes with low to medium device count (GaAs, InP) [1]. Clock (and data) recovery is a key component for any kind of serial data communication and has been demonstrated up to 40 Gbit/s [1]. Circuits such as multiplexers have been published with speeds up to 80 Gbit/s, but there is no published report of a clock recovery (CR) circuit operating at more than 40 Gbit/s. In this Letter we demonstrate the feasibility of a phase-locked loop (PLL) concept for clock recovery at a data rate well above 40 Gbit/s, thus opening a path towards future 80 or 100 Gbit/s circuits. Our approach is to apply a fully analogue PLL topology using an in-house InP/InGaAs-heterojunction bipolar transistor (HBT) process [2] to realise circuits at data rates of 29, 39 and 56 Gbit/s by adjusting particular layout elements.

Modelling: Circuit design and layout were carried out using a commercial simulator with standard Gummel-Poon models for the HBTs, microstrip line models for short interconnects and coplanar waveguide models (CPWs) for both long connections ($>100 \mu\text{m}$) and the resonator of the voltage-controlled oscillators (VCOs). We developed a geometrically scalable, lumped model for metal-insulator-metal (MIM) capacitors and adjusted the built-in models for microstrip lines and coplanar waveguides such that we achieved a fully scalable library of passive elements at the time of the design. All models showed excellent agreement with s-parameter measurements of explicitly designed devices on a number of previously produced wafers and were used to set the centre frequencies of the VCOs (thus the bit rates of our CR circuits) to the desired values in the first design cycle.

Circuit design: Fig. 1 shows the topology of the present CR-PLL which is also a major part of a future quadricorrelator circuit: the data input is followed by a buffer amplifier converting the single-ended input to a differential signal. All the following blocks make use of a fully differential topology. The block denoted 'DRML' (a stacked modified Gilbert-Cell proposed by Razavi [3]) performs capacitive differentiation ('D'), rectification ('R'), mixing with the