Nanoparticle Memories: CMOS, Organic and Hybrid approaches

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"Winter School on Nanoelectronic and Nanophotonics"

Bilkent University

Ankara, Turkey

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Outline

- 16:00 – 16:50 (3rd Hour)

  NP-NVM: Hybrid approach
  - Si/Organic hybrid technology
  - Principle of operation
  - Demonstrators: NP in Hybrid Si/Organic memory devices

  NP-NVM: Organic approach
  - Organic electronics
  - Principle of operation
  - Demonstrators: NP in Organic memory electronics

Combination of functional Organic – Inorganic materials

- Why Organic materials?
  - Low-temperature integration process
  - Plurality of materials to select
  - Flexibility to modify their structure and physico-chemical properties
  - Compatible with NPs and self-assembly techniques
  - Easy deposition techniques and good enough thickness control in nanometer scale (experience integration of low-*k* materials in CMOS fabrication processes)

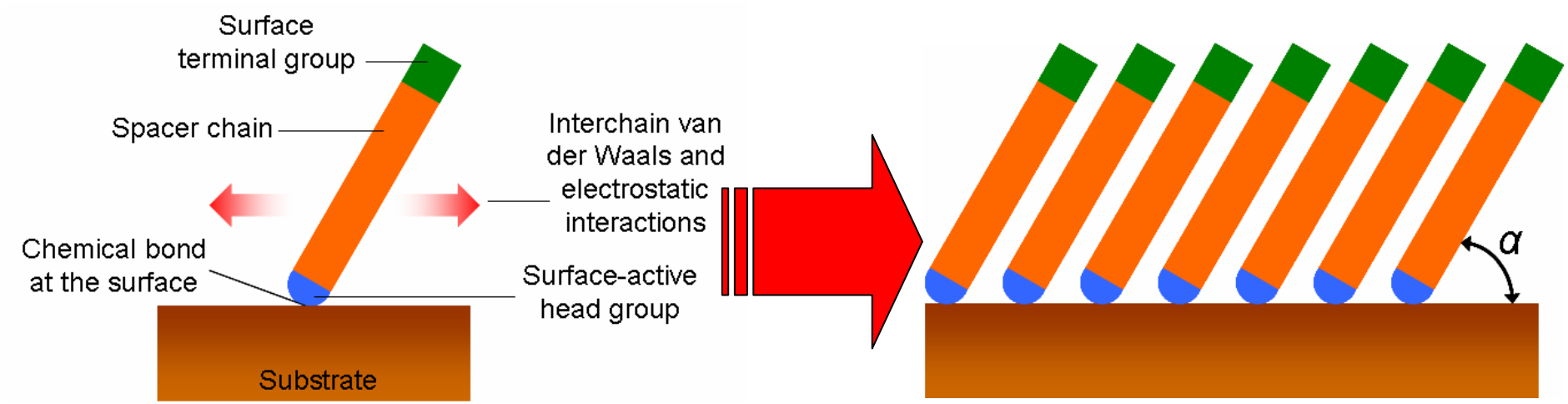
Organic materials can be used to answer several NP-NVM issues.

Deposition of self-assembled nanoparticles

- Overcome the large variation in size, shape *etc* distributions of NPs self-assembly techniques might be used.
- Self-assembly techniques offer sub-lithographic features
- Self-assembly techniques
  - Deposition on SAMs
  - Langmuir-Blodgett (LB)
  - Layer-by-layer (LBL)
  - etc
- NPs Self-assembly process require
  - Ex-situ synthesis of NPs having uniform size
  - Functionalization of NPs
  - Selective deposition of NPs
  - Functionalization of deposition surfaces

Self-assembled monolayers (SAMs)

- SAM properties are determined by terminal and head groups.
  - Terminal group: Surface energy (low & hydrophobic, high & hydrophilic), anchor for specific overlayers
  - Head group: exothermic bond with substrate, molecules try to occupy any available binding site
  - Chain: alkyl or derivatized alkyl group, tilt angle (e.g. 55-60° for Au and alkanethiolate)



SAMs and Surface functionalization

- Terminal groups – Hydrophilic
  - Alcohol (-OH)
  - Carboxylic acid (-COOH)
- Terminal groups – Hydrophobic
  - Methyl ($-CH_3$)
  - Trifluoromethyl ($-CF_3$)

- Surface-active head groups – Metal
  - Thiol (-SH)
- Surface-active head groups – Si or SiO_2
  - Silane ($-SiH_3$)
  - Trichlorosilane ($-SiCl_3$)

Alkanes
Alkenes
Aromatic hydrocarbons
Ethers
Aldehydes, ketones, carbonyls
Thiols
Amines
Alcohols, phenols
Amides
Carboxylic acids

Polarity ↓

Hydrophobicity ↑

```
H   H   H
|   |   |
– Si – Si – Si –
```

HF treated Si

```
OH  OH  OH
|   |   |
– Si – Si – Si –
```

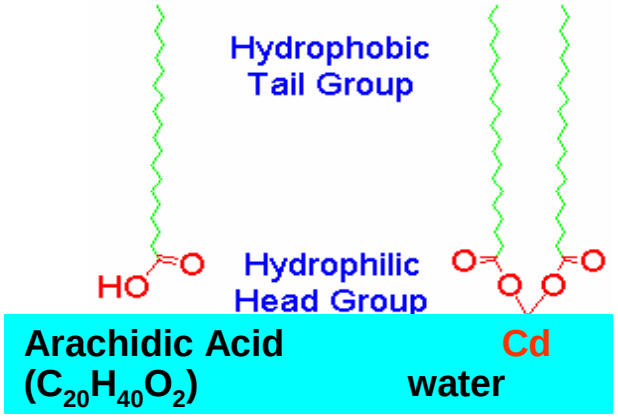
Piranha treated Si

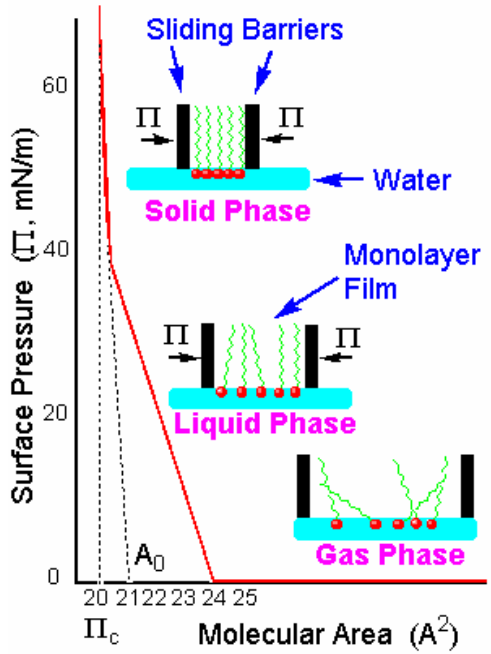
```
|   |   |
O   O   O
|   |   |
– Si – O – Si –
```

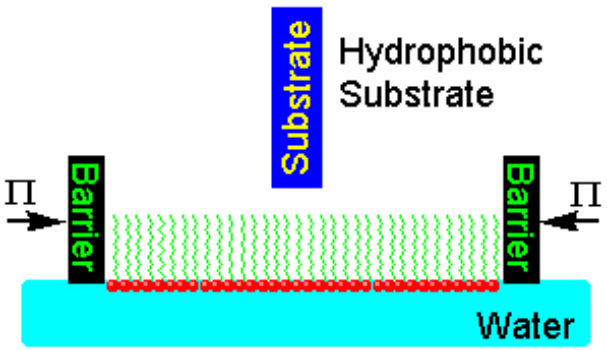
O plasma treated Si

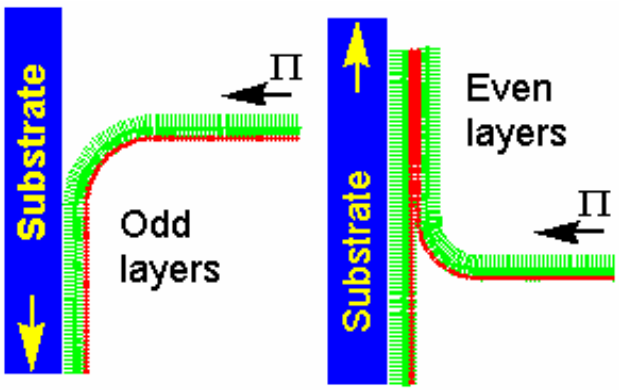
LB technique

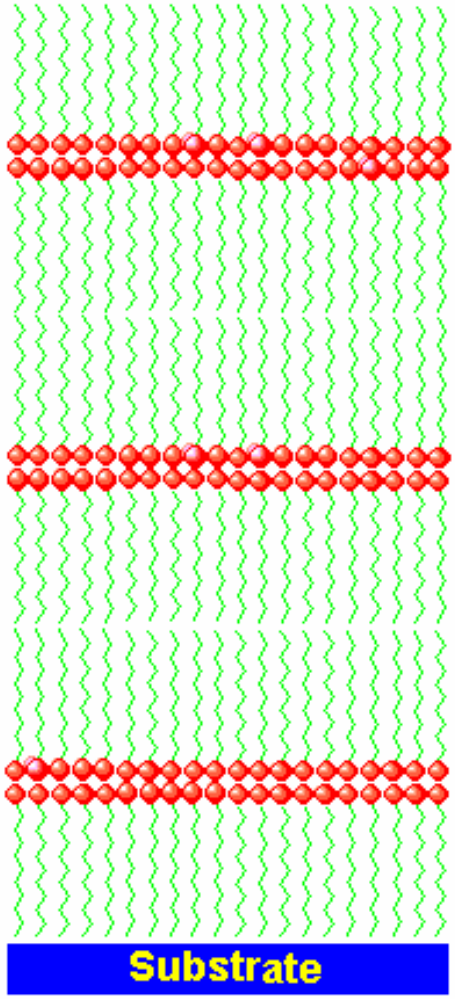
- (Multi)Layer deposition on any substrate





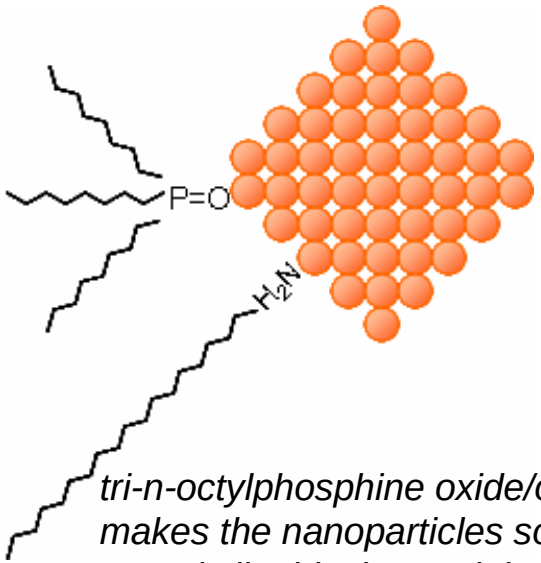




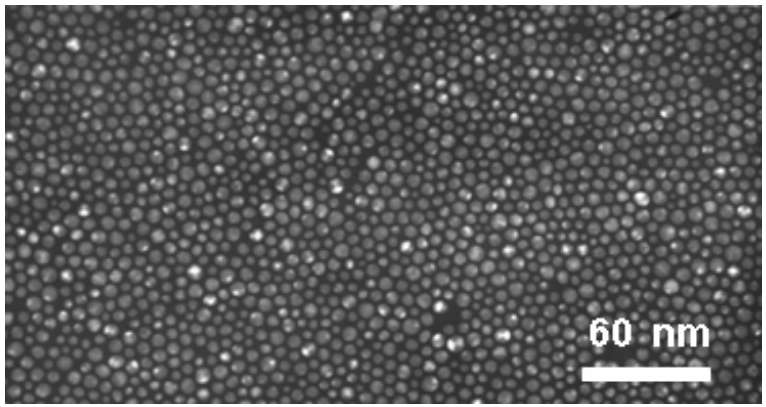


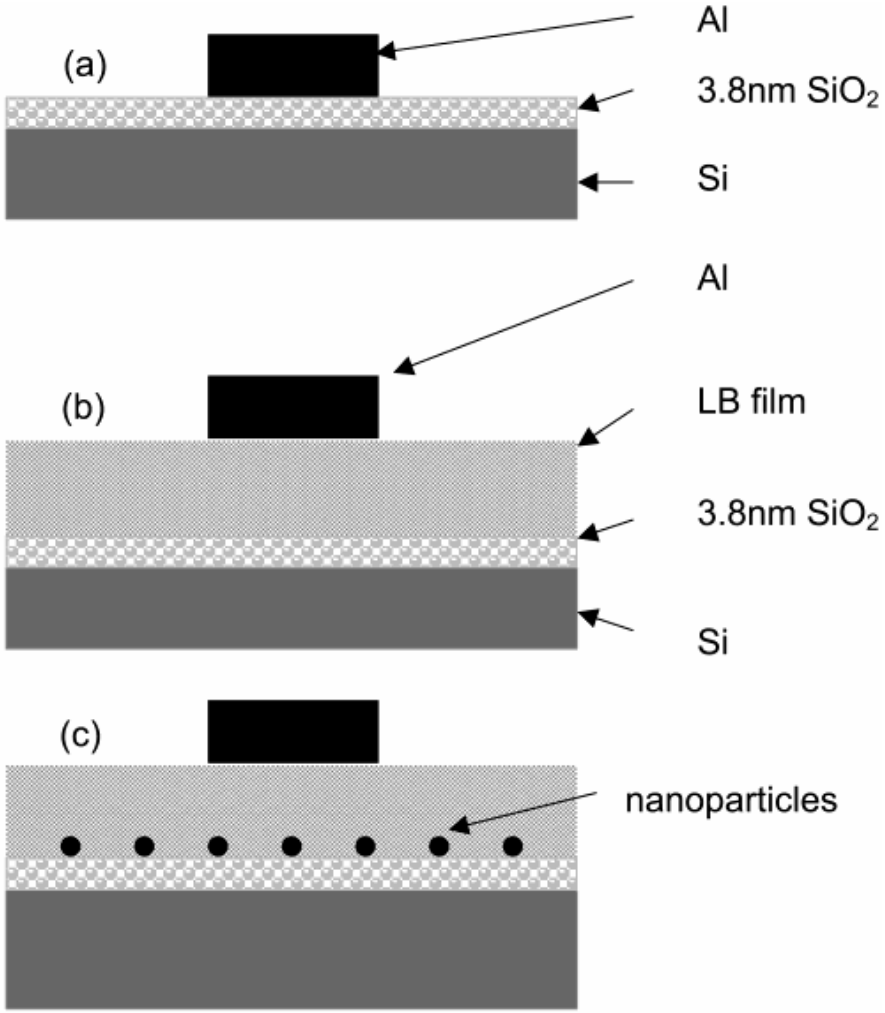
LB Hybrid capacitor memory cells

- LB technique is used to deposit (a)Au-NPs on SiO2 and (b)organic dielectric layer acting as blocking layer



tri-n-octylphosphine oxide/octadecylamine: makes the nanoparticles soluble in various organic liquids, but mainly insoluble in water

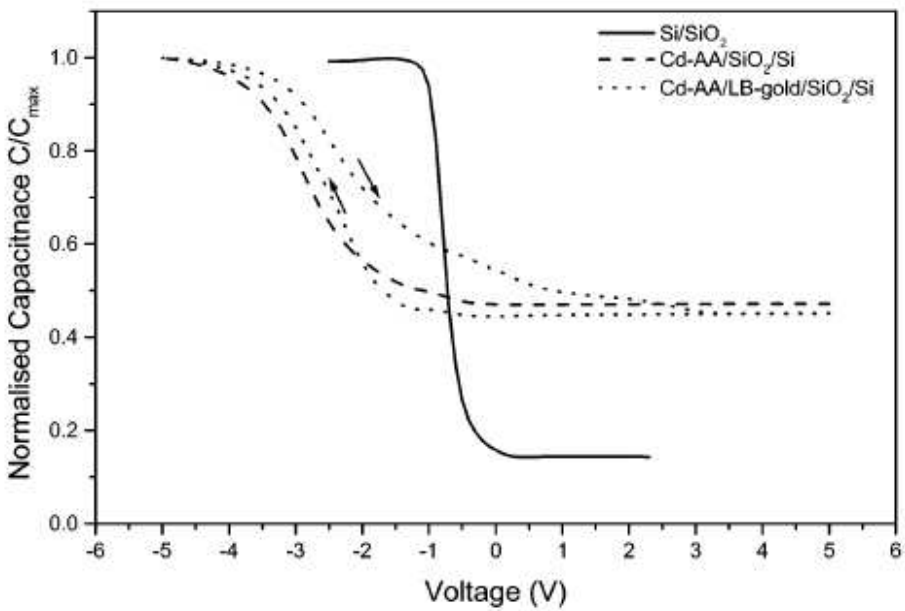


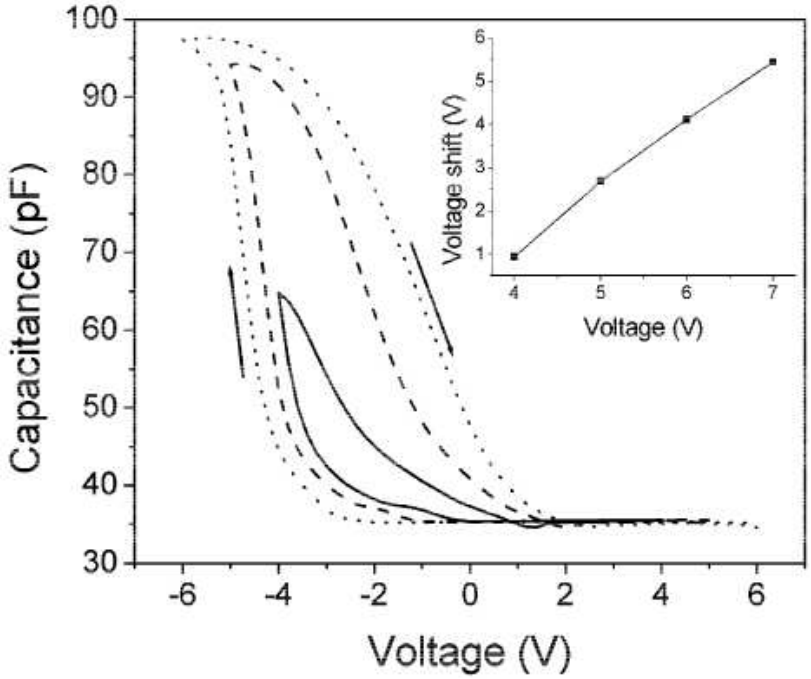


*S.Paul et al., NanoLetters **3**, 533 (2003)*

LB Hybrid capacitor memory cells

- Comparison between control samples and Au-NPs
- C-V measurements for charge storage and memory window identification



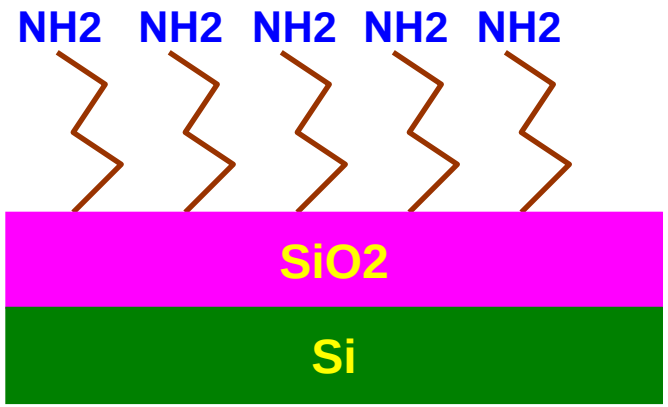


The observed C-V hysteresis is clockwise denoting that the charge exchange takes place between the Au-NPs and the metal gate.

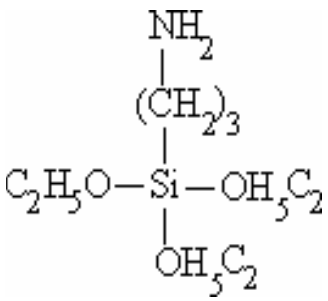
Direct self-assembly of Au-NPs

- Substrate functionalization

1ml APTES : 9ml toluene



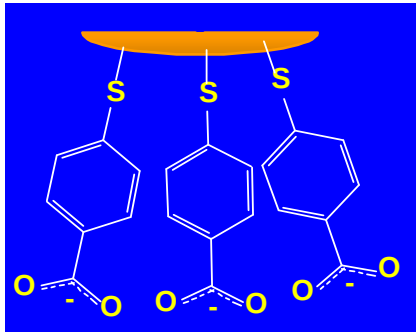
3-aminoPropylTriEthoxySilane



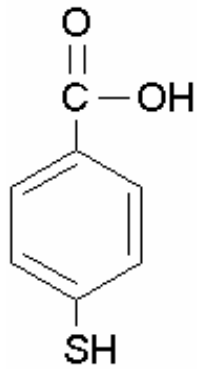
- Au-NPs functionalization

Functionalized (acid-derivatized) Au-NPs

4-mercaptobenzoic acid : $NaBH_4$: $HAuCl_4$

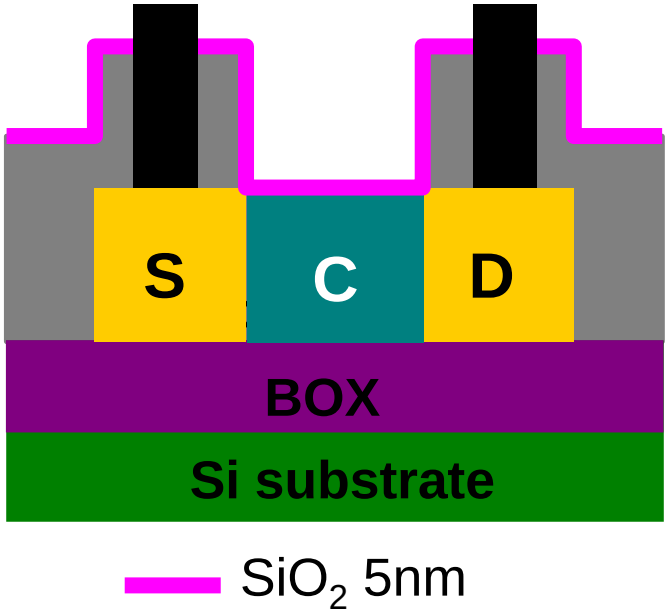


4-mercaptobenzoic acid

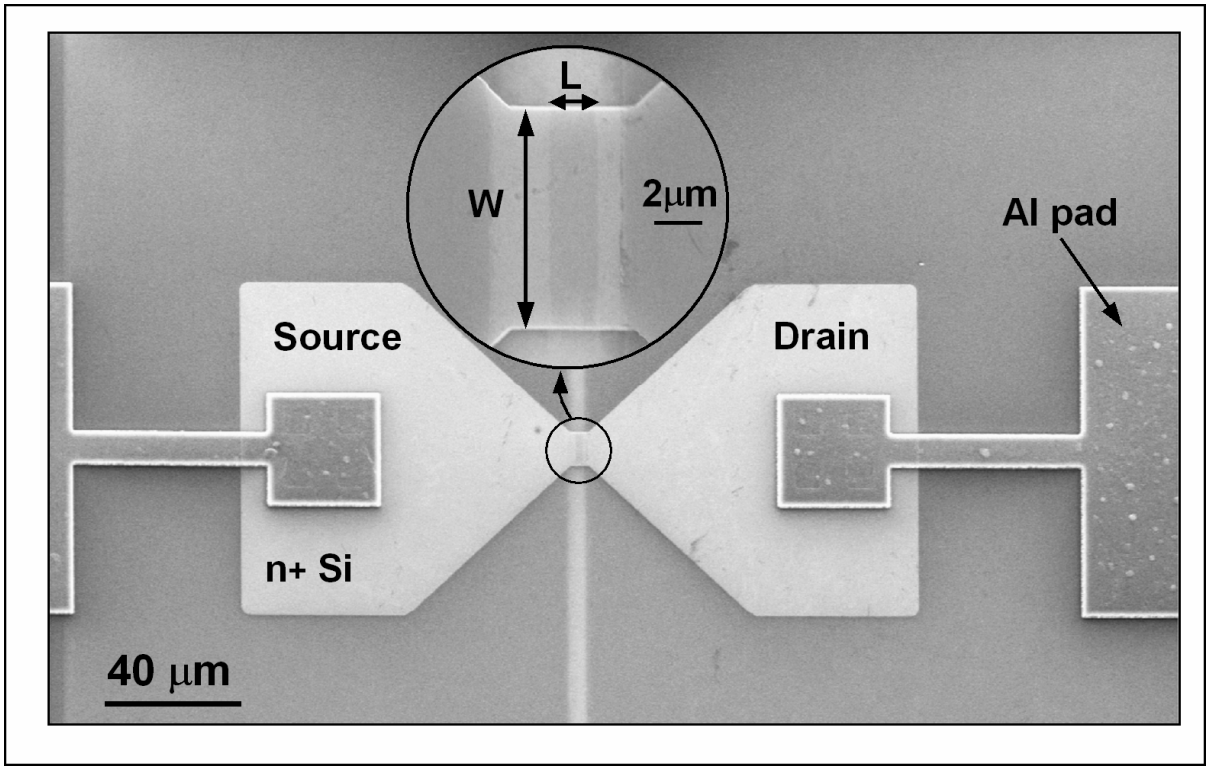


Hybrid FET with Au-NPs

- IMEL CMOS SOI 0.8 – 2 μm

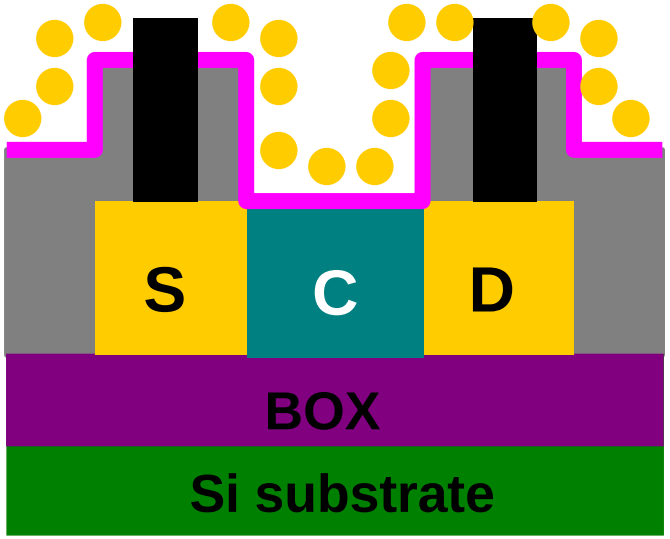


SEM image of the fabricated FET on SOI substrate



Hybrid FET with Au-NPs

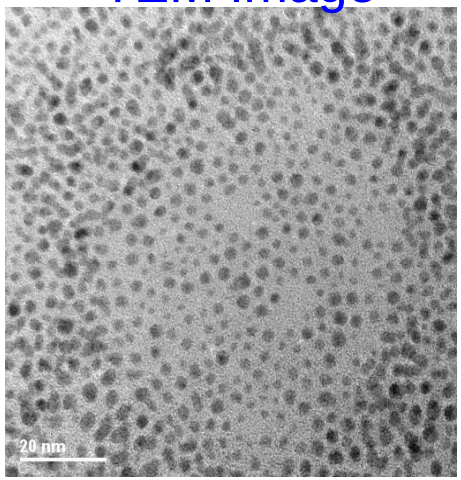
- Direct self-assembly of Au-NPs on the gate insulator of an SOI FET



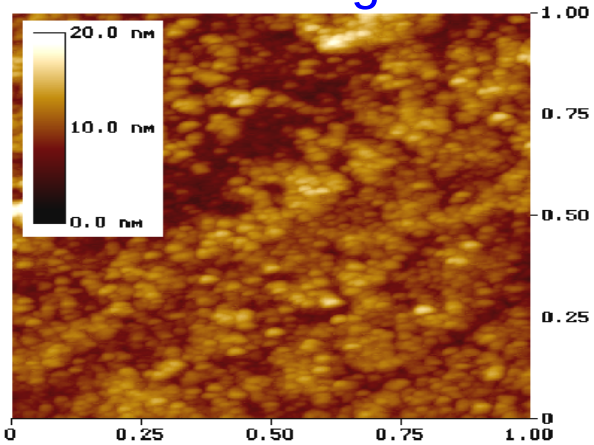
Au-NPs : ~5nm
~5x10^{12} cm^{-2}

- Direct self-assembly of Au-NPs on the gate insulator of an SOI FET

TEM Image



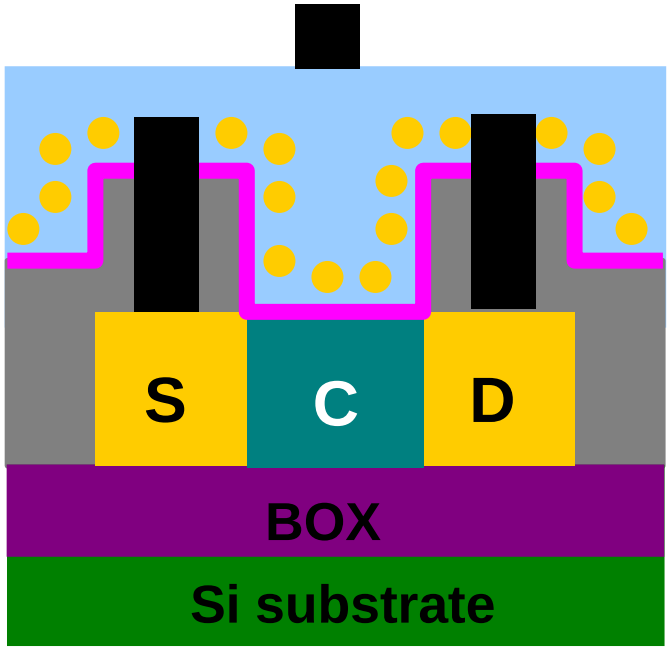
AFM Image



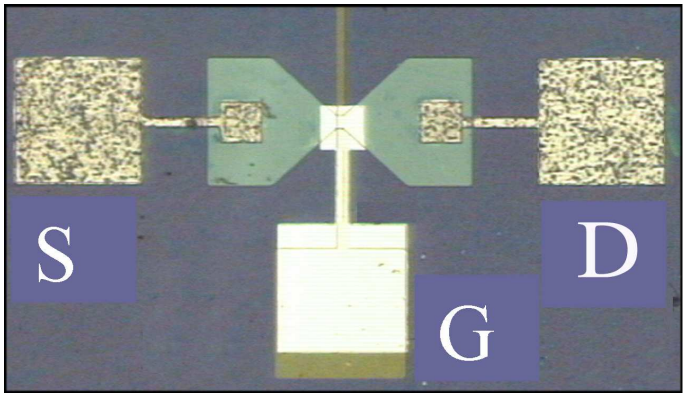
Kolliopoulou et al ESSDERC 2003

Hybrid FET with Au-NPs

- LB deposition of Organic blocking dielectric



- Au-NPs covered by 20 monolayers (54nm) of $C_{20}H_{38}O_2Cd$ (Cadmium Arachidate, *k*=2.6)



- Al patterning by developer AZ726 (using AZ5214 positive)

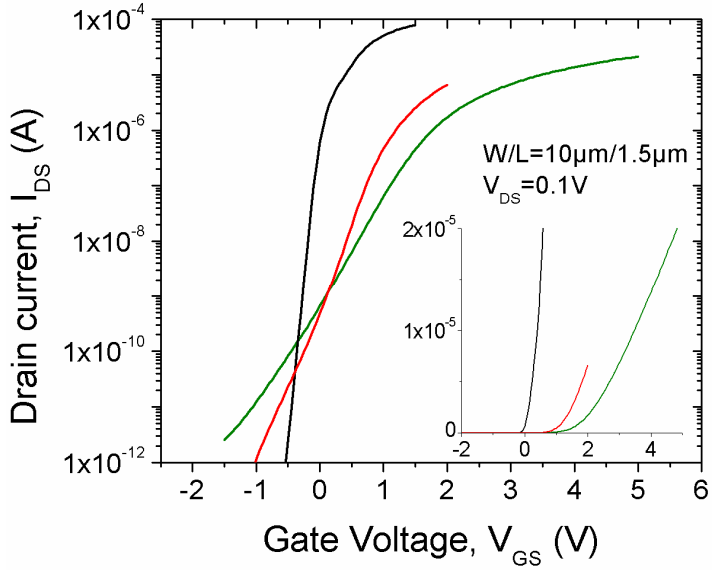
*Kolliopoulou et al, ME **73-74**, 725 (2004)*

Hybrid FET with Au-NPs

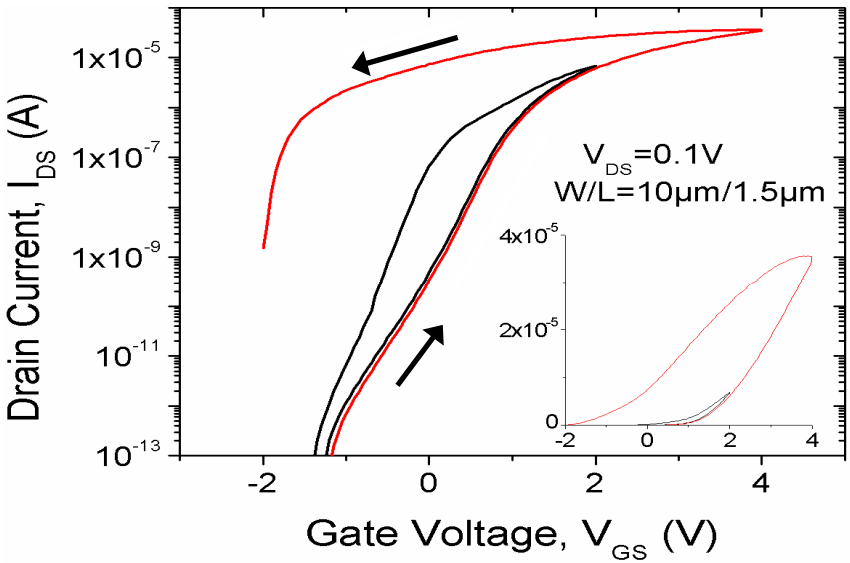
- Electrical characterization

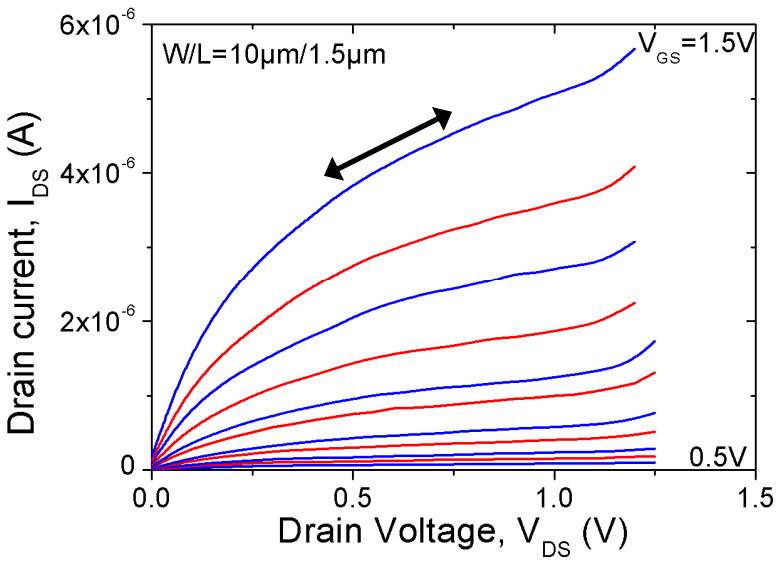
Subthreshold slope is affected by processing steps and additional layers

- Reference (SiO_2 insulator)
- Insulator Stack (LB/SiO_2 insulators)
- Memory Stack (LB/Au-nps/SiO_2)



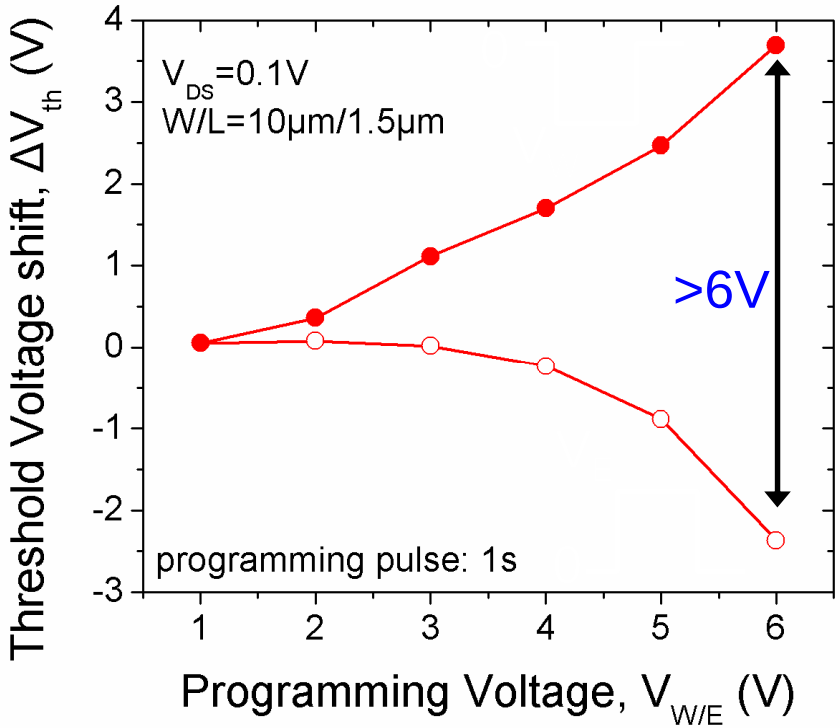
I-V hysteresis is clockwise (charge exchange from the gate metal)

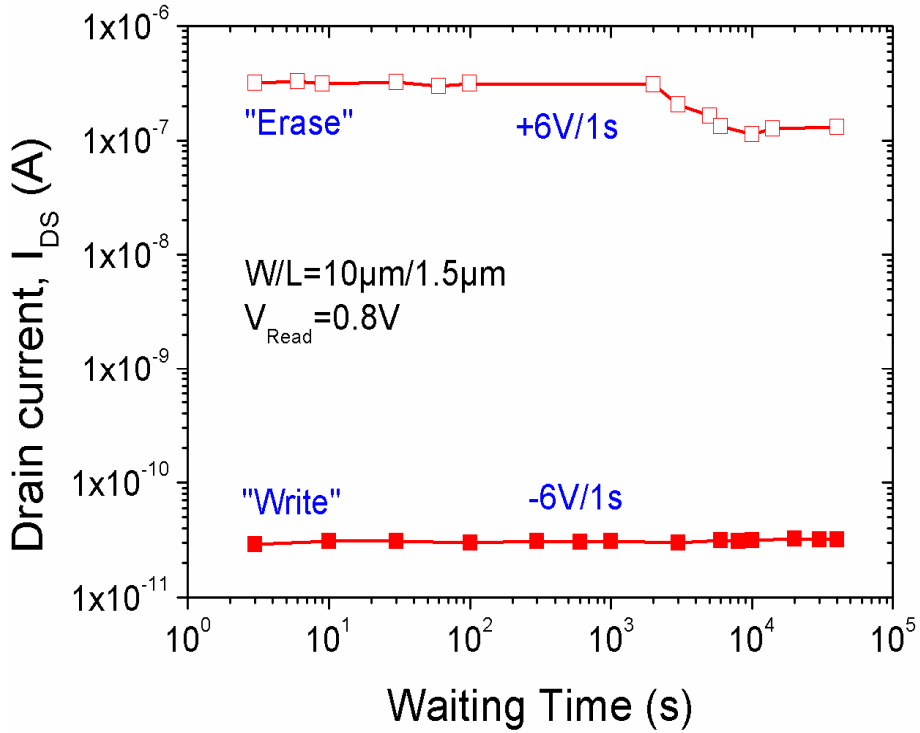




Hybrid FET with Au-NPs

- Charge storage and memory window characterization



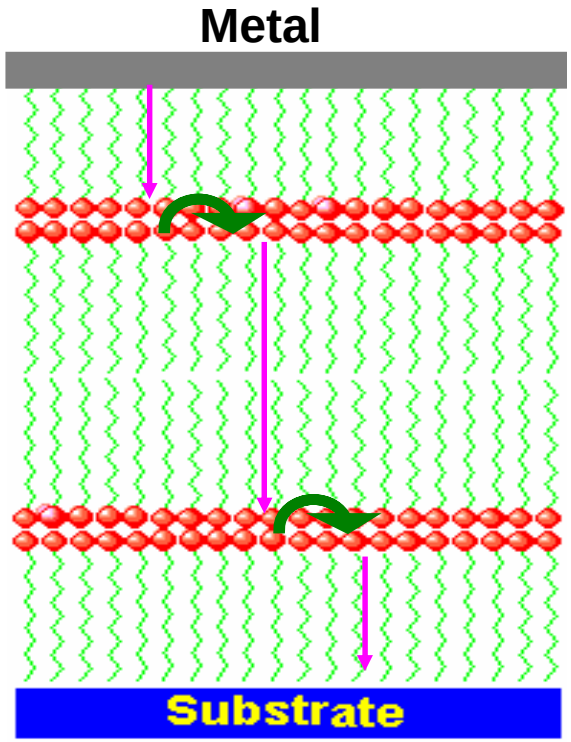


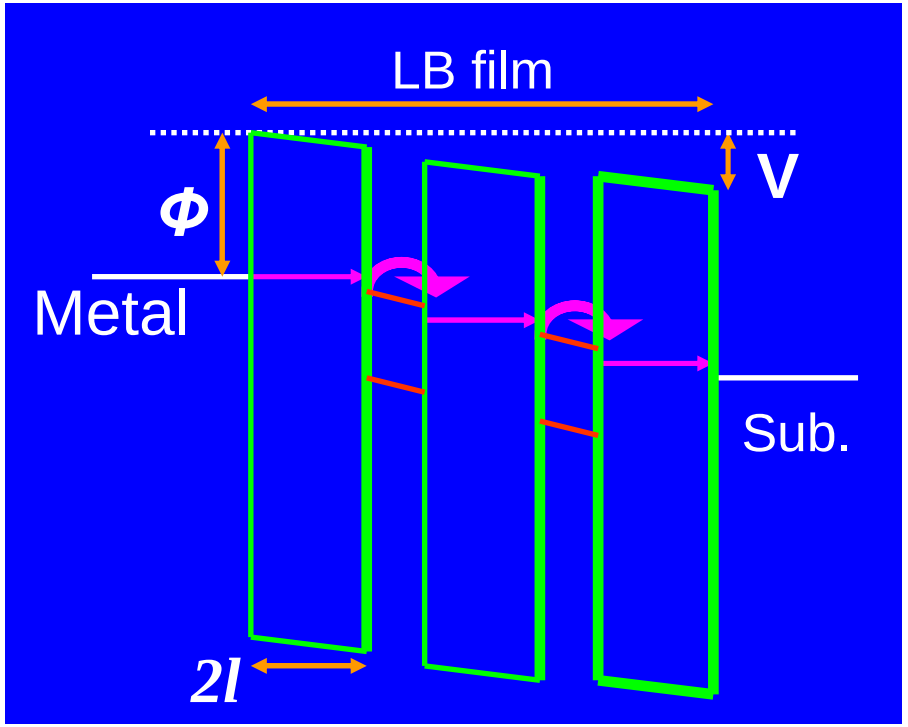
- PGM: V_G<0, ERS: V_G>0 (≥ 1s)
- Dielectric degradation
- Retention: 11h

Kolliopoulou et al. JAP 94, 5234 (2003)

Hybrid FET with Au-NPs

➢ Gate leakage through LB dielectric layers





- Electron tunneling through the LB bilayer
- Thermally activated hopping within the plane of carboxylic head groups

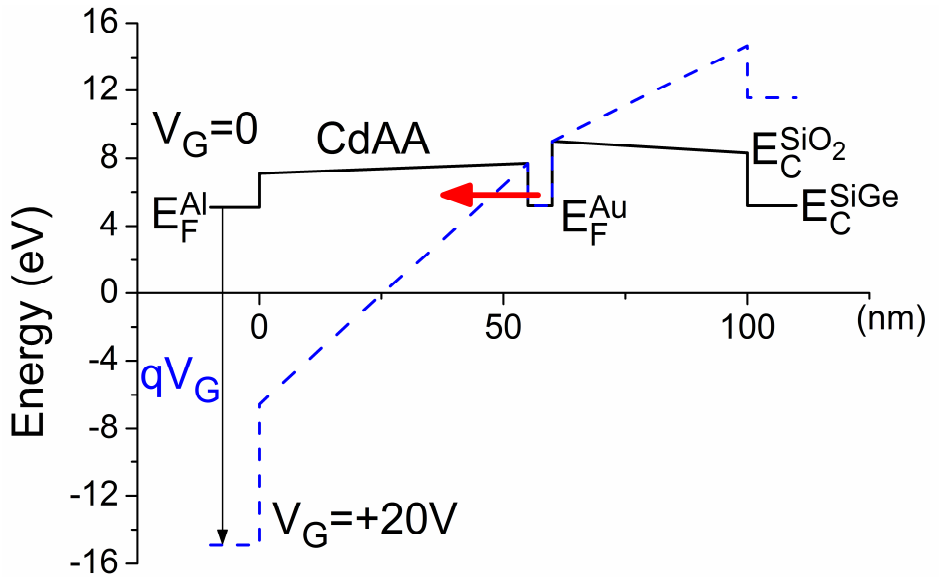
$$\lambda = \lambda_0 (2\alpha l)^{\frac{3}{2}} \exp\left[-(2\alpha l) - \left(\frac{4\alpha}{\pi N_t l k T}\right)^{\frac{1}{2}}\right]$$

*Nabok et al. MSE C **22** (2002) 355*

Hybrid FET with Au-NPs

➢ Energy band diagram

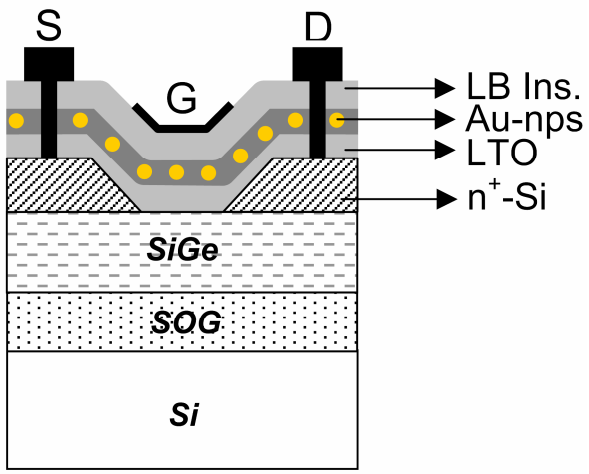
Material	Φ (eV)	χ (eV)	φ_{SiO2} (eV)	φ_{CdAA} (eV)
SiGe	4.1		3.1	
SiO_2		1.0		
LB CdAA		2.3		
Al	4.2		3.2	2
Au	4.8		3.8	2.5



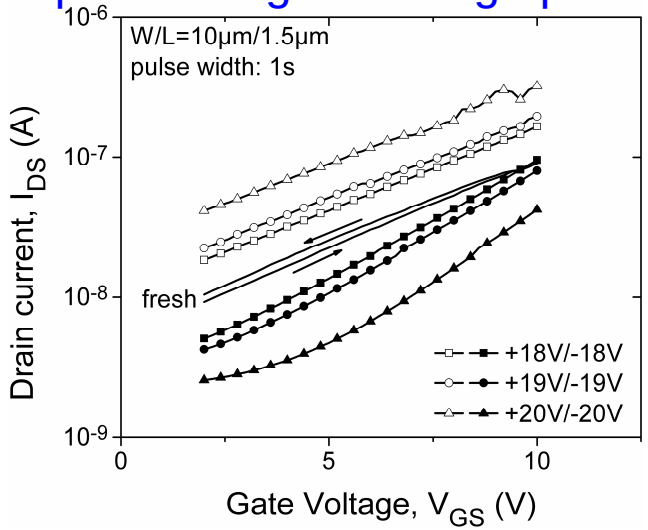
*Kolliopoulou et al, ME **83**, 1563 (2006)*

Hybrid FET with SiGe channel & Au-NPs

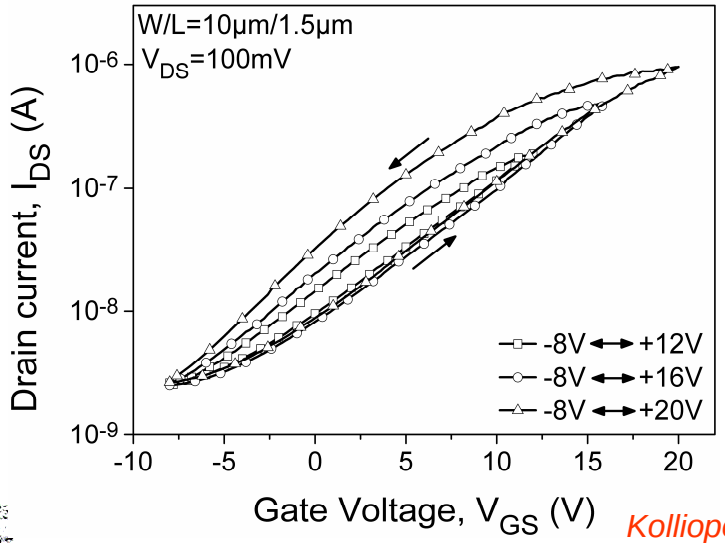
➢ Wafer bonding – SiGe channel FET memory cell



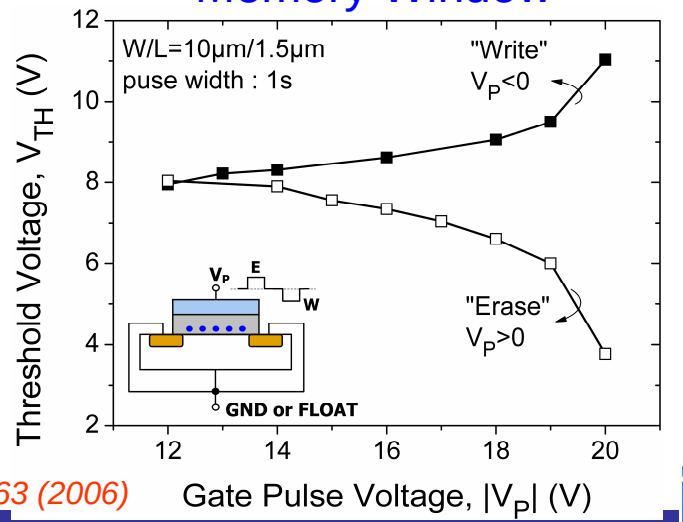
Response on gate voltage pulse



Transfer characteristics – *I-V* Hysteresis



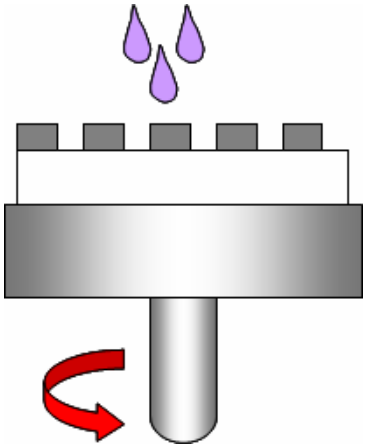
Memory Window

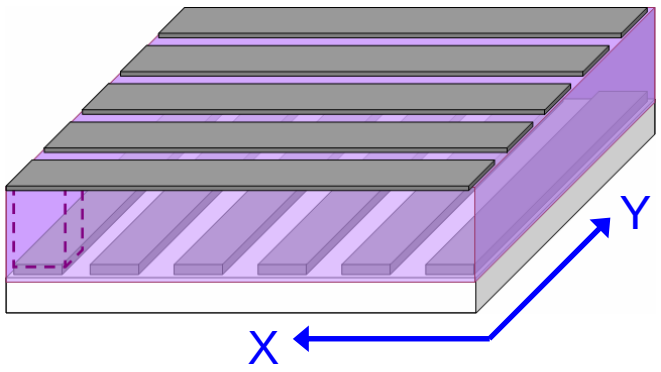


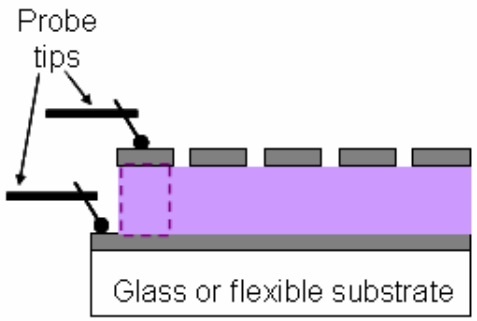
*Kolliopoulou et al, ME **83**, 1563 (2006)*

Two terminal Organic memory cells

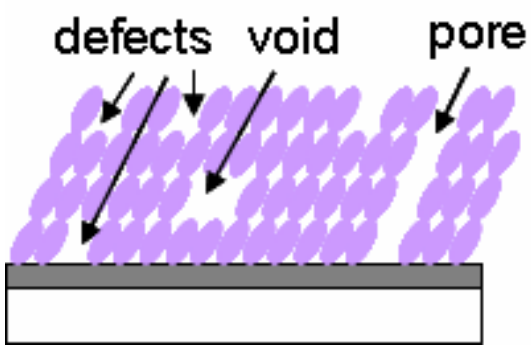
- Cross-point architecture (solution processed devices-spin coated)



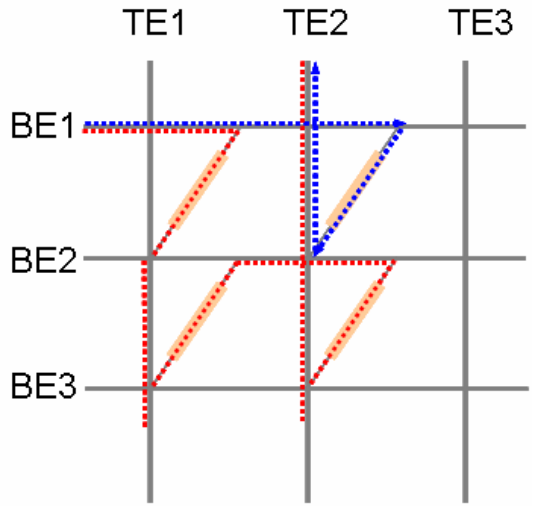




- Main fabrication issues



Read (BE1, TE2)
Direct current
Leakage current

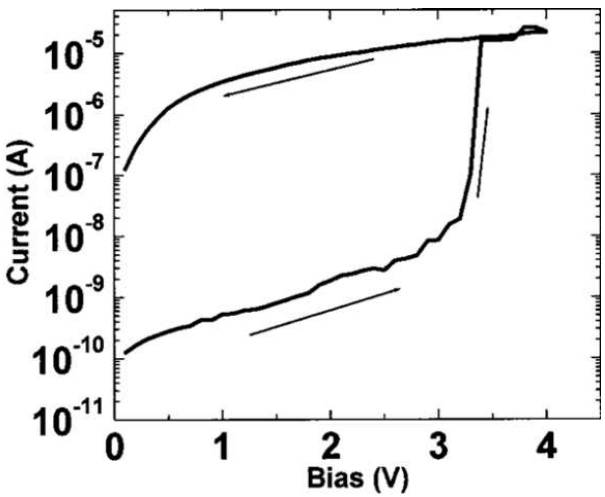


Organic films with embedded NPs (Blends & sandwiches)

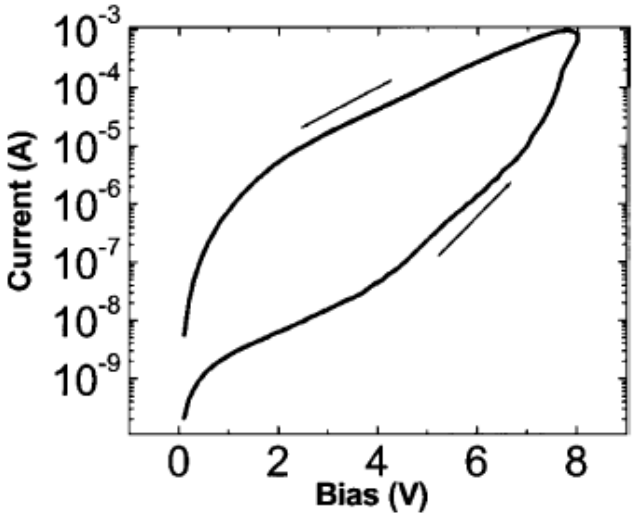
- Metal NPS cause organic layer's conductivity to switch between a high and a low value

Functionalization of Au-NPs

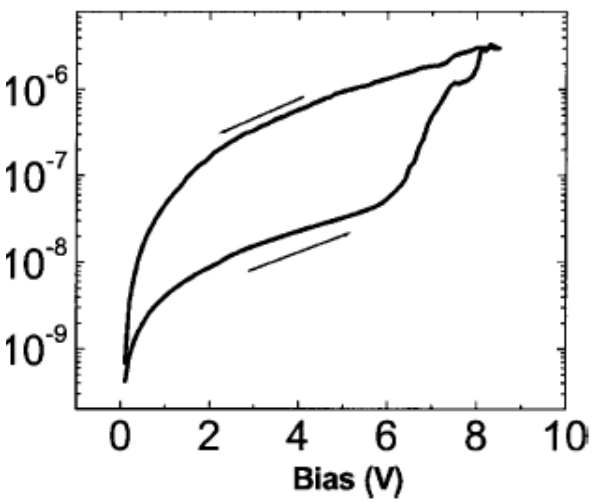
- 1-dodecanethiol (DT)
- 2-naphthalenethiol (2NT)
- 2-benzeneethanethiol (BET)



Al / NPB / Au-DT NP+8HQ+PS / Al / glass



Al/Au-2NT NP+PS/Al

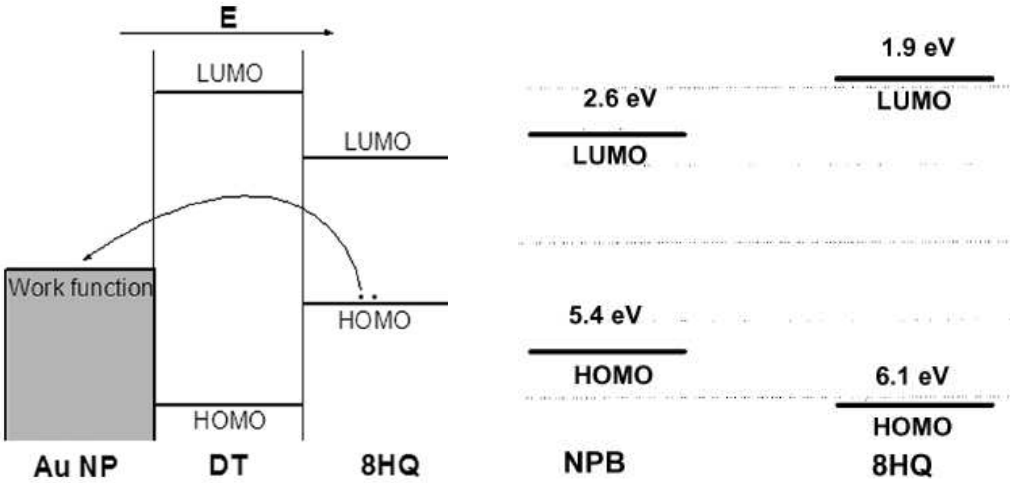


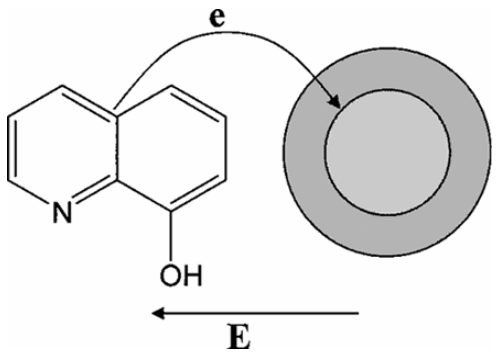
Al/Au-BET NP+PS/Al

J.Ouyang *et al.*, Proc IEEE 93, 1287 (2005)

Organic films with embedded NPs (Blends & sandwiches)

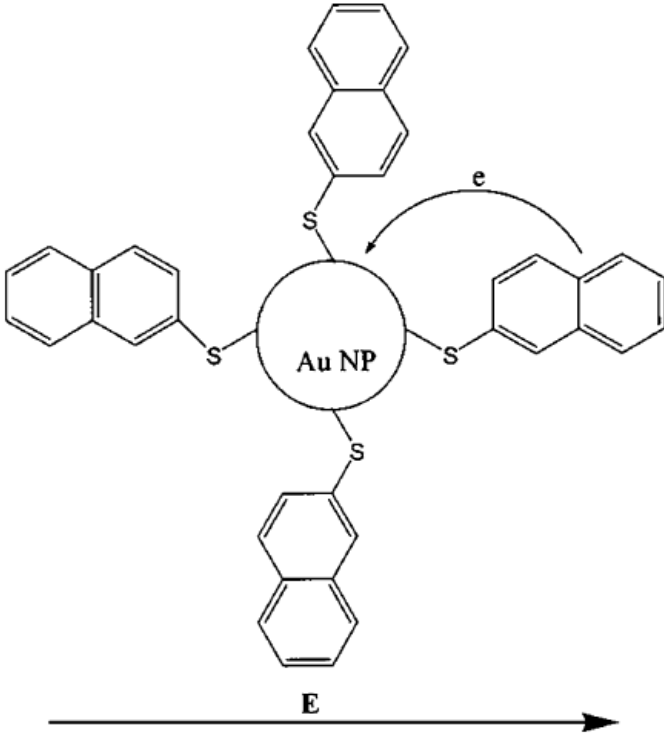
- Charge exchange mechanisms





Al / NPB / Au-DT NP+8HQ+PS / Al / glass

Al/Au-2NT NP+PS/Al

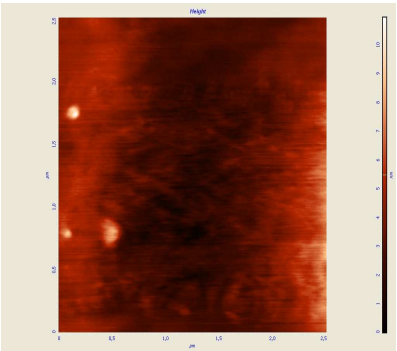


Al/Au-BET NP+PS/Al

Al / Cu-NPs + P3HT / Al

- Evaporation of Cu on P3HT and vacuum annealing

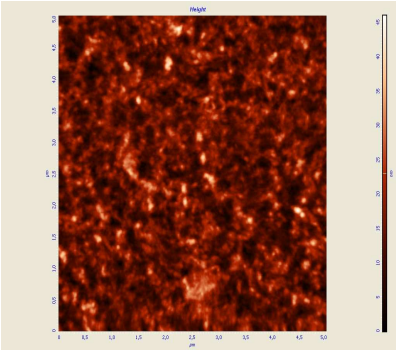
P3HT on Quartz



Uniform P3HT layer

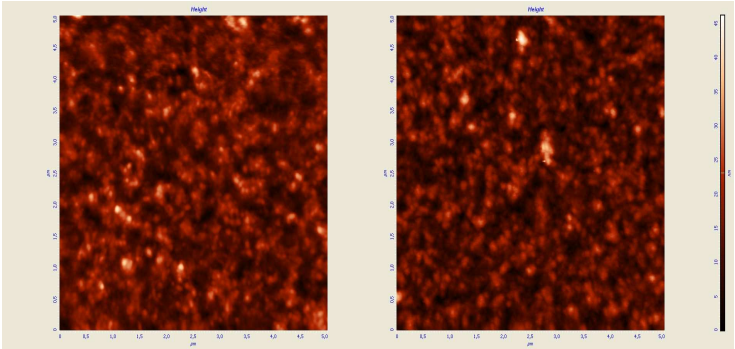
As-coated

Cu on P3HT

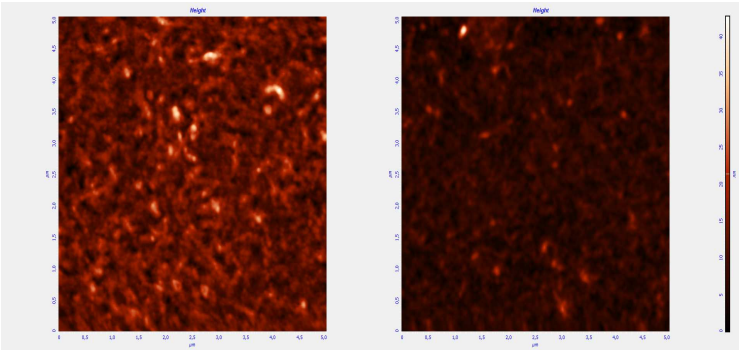


Cu precipitates on P3HT layer

As-deposited



125°C / 10min 125°C / 30min

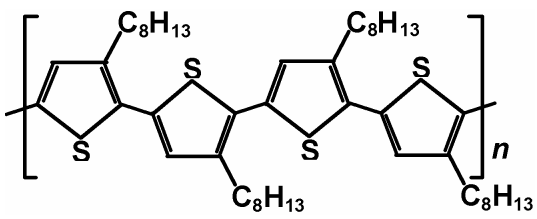


155°C / 10min 155°C / 30min

P.Dimitrakis et al., E-MRS 2008

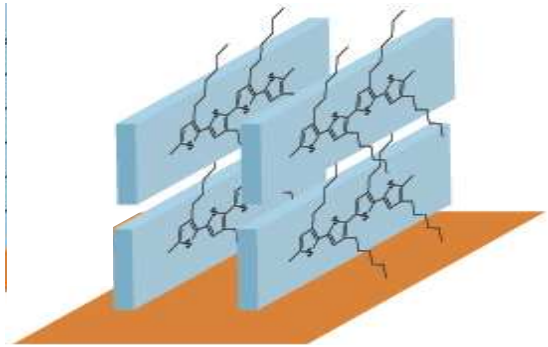
Al / Cu-NPs + P3HT / Al

- P3HT and Cu NPs memory cells

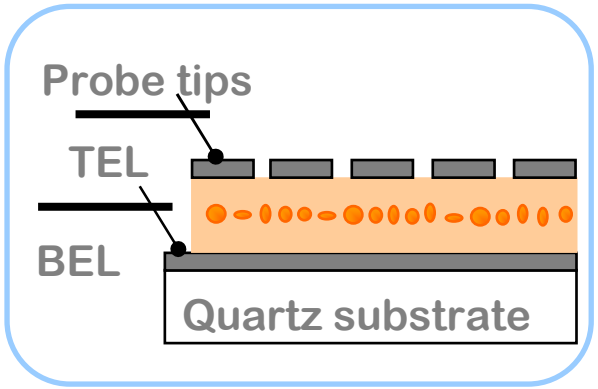


P3HT

P.Dimitrakis et al., E-MRS 2008



RR-P3HT stacking

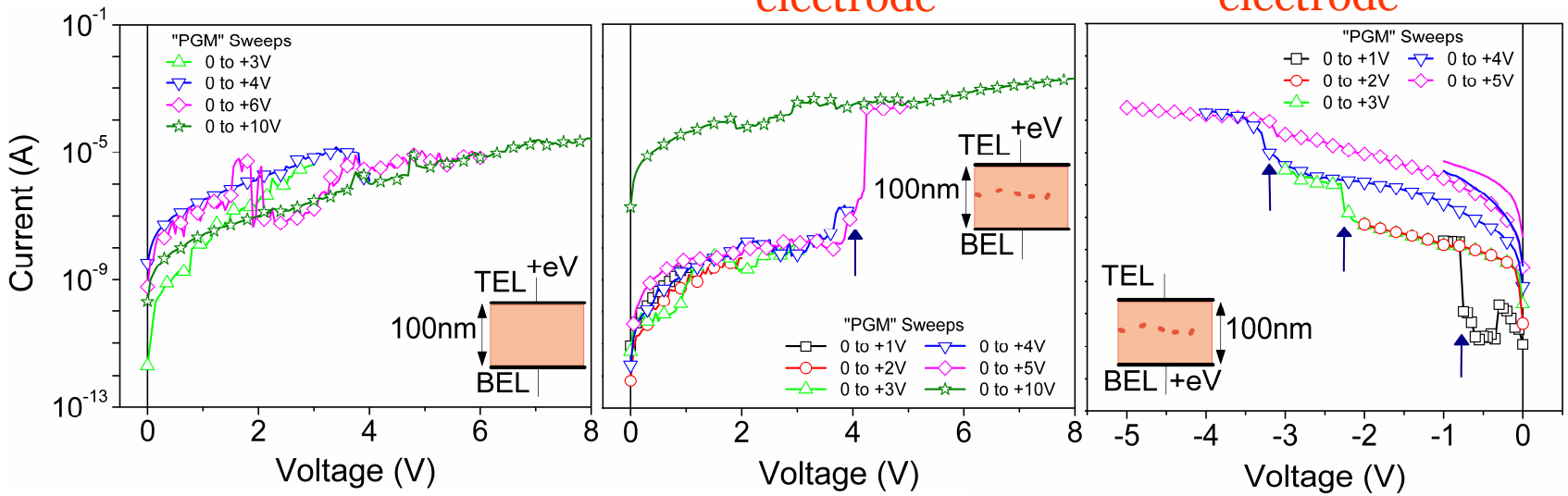


Probes arrangement for electrical characterization

A. Control Device

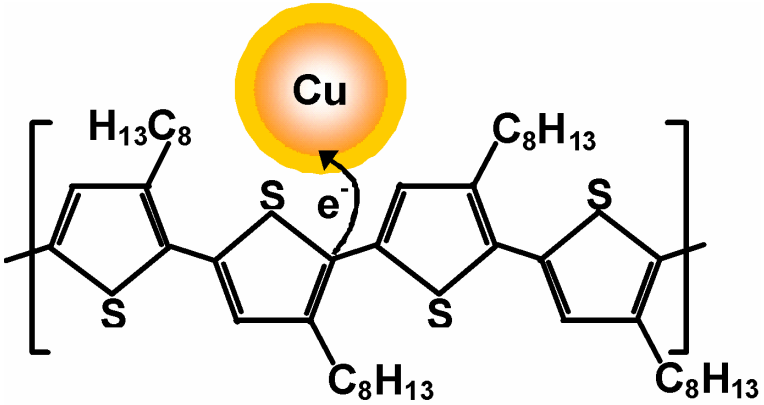
B. BEL as ground electrode

C. TEL as ground electrode



Al / Cu-NPs + P3HT / Al

- Proposed mechanism



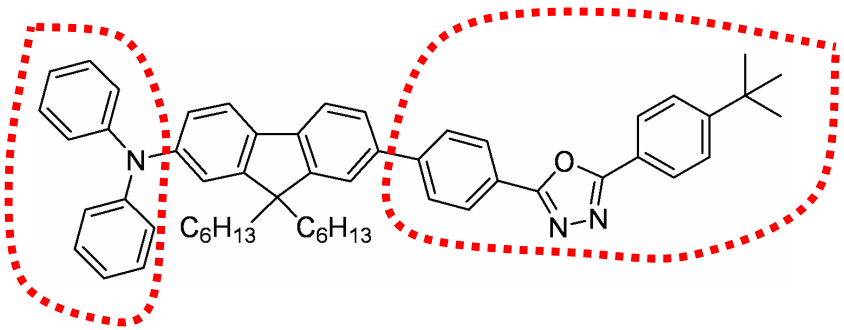
When the electric field increases to a certain value (switching voltage), electrons on the highest occupied molecular orbital (HOMO) of P3HT may gain enough energy to tunnel through the outer oxide into the Cu-NP.

Consequently, the HOMO of P3HT becomes partially filled (i.e., P3HT is charged positively) whereas Cu-NP is charged negatively. The above mechanism is proposed to explain carrier generation resulting to a high-conductivity state.

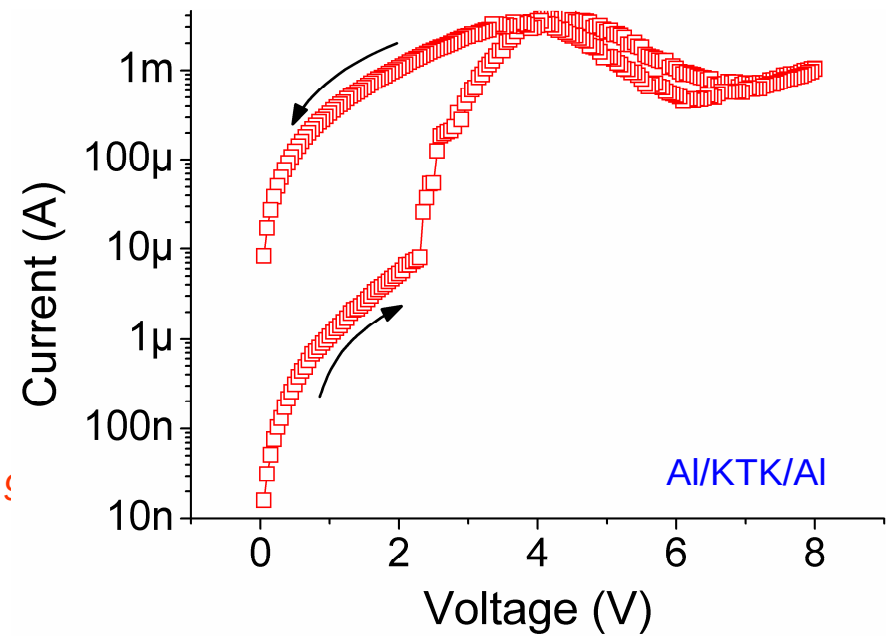
P.Dimitrakis et al., E-MRS 2008

Unipolar operation of 2-terminal MOM cells

- Metal/Organic/Metal devices in cross-bar architecture exhibit NDR regions in I-V characteristics
  - Trapping at Defects (charge screening effect)
  - Metal Filaments (diffusion of metal atoms from electrodes)



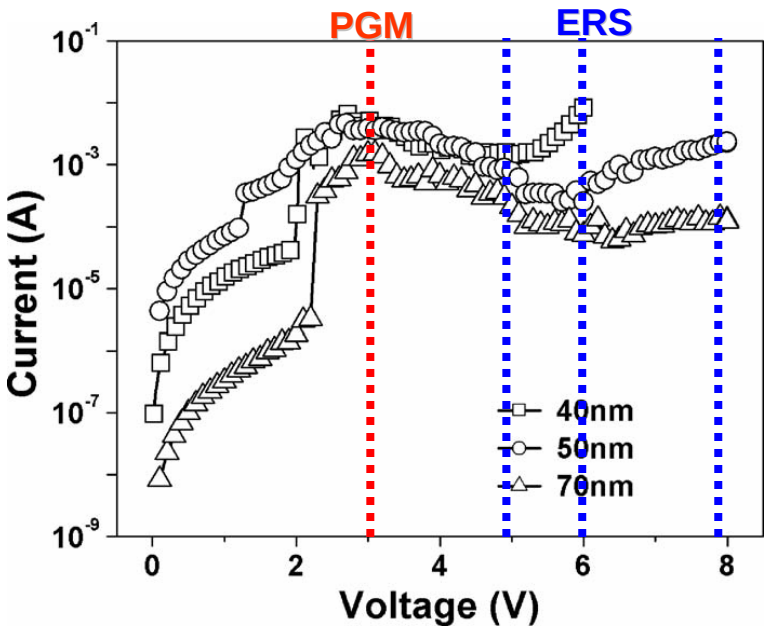
C. Pearson et al., UK Patent Application No. 0703864.9 pending

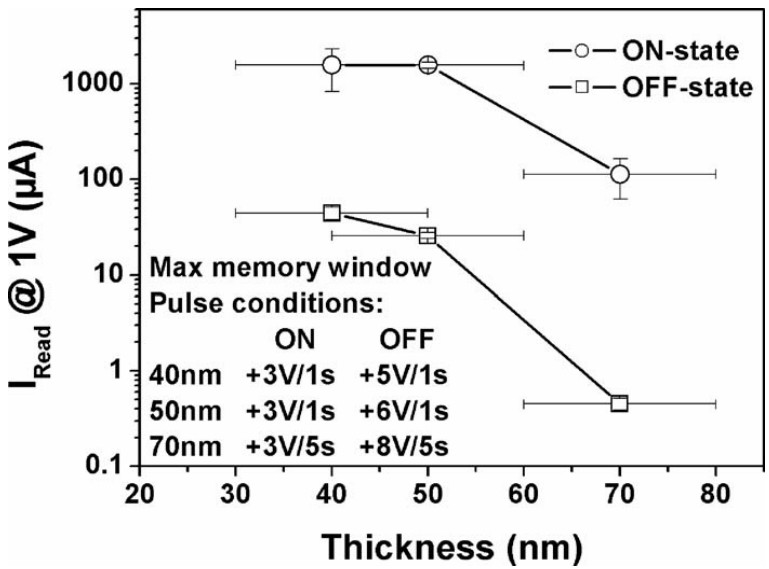


*C. Pearson et al., APL **91**, 123506 (2007)*

Enhanced Unipolar operation of MOM + Au-NPs cells

- Organic blends: KTK + 0.5% Au-NPs (I_{ON}/I_{OFF}>100)





Bibliography

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