# Nanoparticle Memories: CMOS, Organic and Hybrid approaches

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IMEL/NCSR "Demokritos"

"Winter School on Nanoelectronic and Nanophotonics"

Bilkent University

Ankara, Turkey

19-25 January 2009

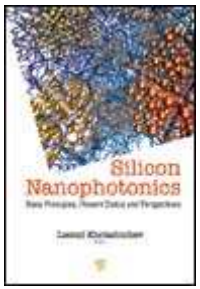
# Outline

- 14:00 – 15:50 (2nd Hour)

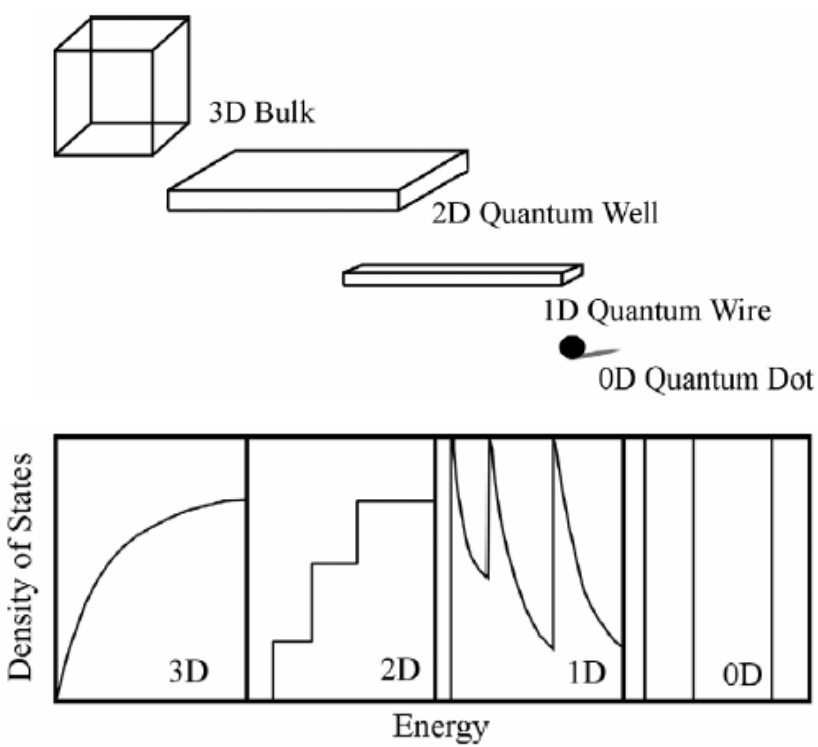
  NP-NVM: CMOS Approach
  - Introduction to NP Memory concept
  - Advantages of NP-NVM
  - Fabrication methods in CMOS Environment
  - Electrical characterization methods
  - Optimization – New cell architectures
  - State of the Art

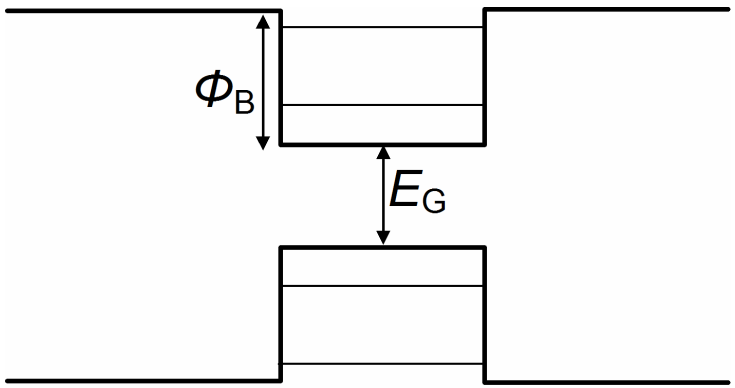
*"Size matters: Why NM are different?" by E. Roduner*
*Chem. Soc. Rev., 2006, 35, 583–592*

*P.Dimitrakis, Chapter 8 in "Silicon Nanophotonics", ed. L.Khriachtchev, 2008*

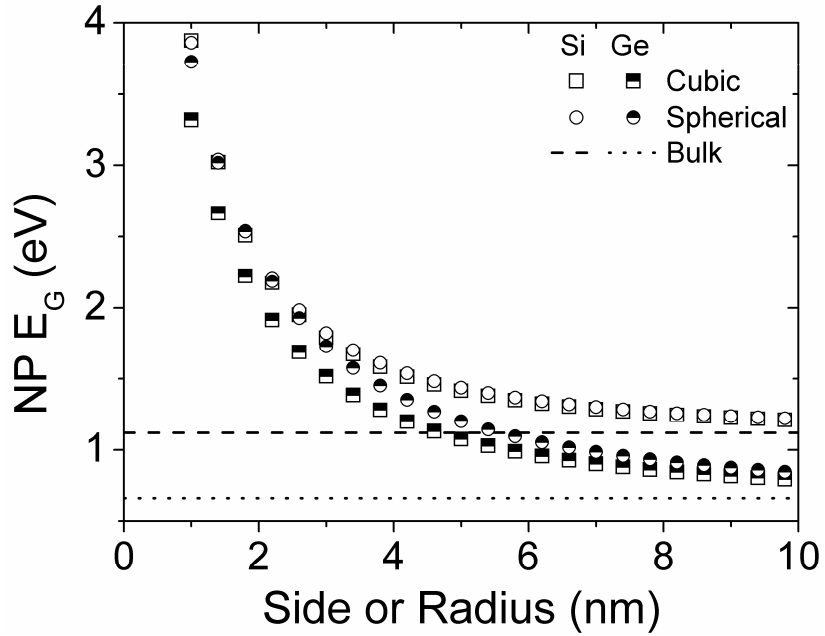


# Introduction to NP Memories: Properties of Semiconductor NP

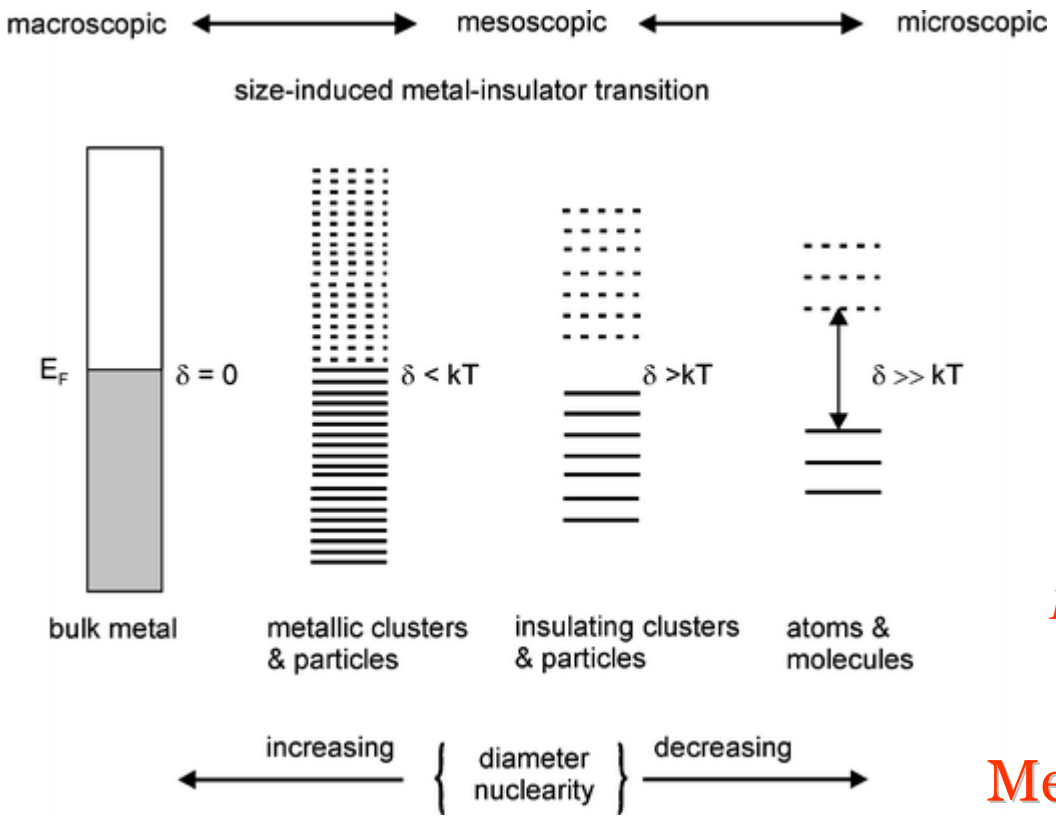



$$\Delta V_{TH} = \frac{q \cdot n \cdot \nu}{\varepsilon_{ctrl}} \left( t_{ctrl} + \frac{1}{2} \frac{\varepsilon_{ctrl}}{\varepsilon_{Si}} t_{nc} \right)$$



# Introduction to NP Memories: Properties of Metal NP




## Kubo gap

$$\delta = 4E_F / 3n$$

- Metallic $k_B T > \delta$
- Insulating $k_B T < \delta$

*R. Kubo, J. Phys. Soc. Jpn.* ***17****, 975 (1962)*

## Metal vs Semiconductor NP

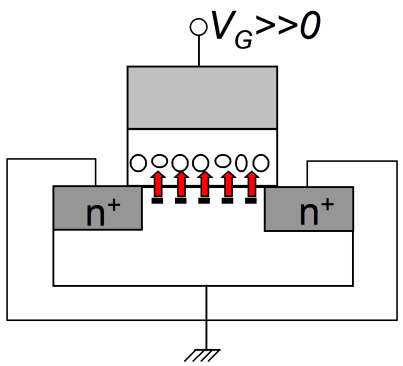
✓ Higher density of states at $E_F$

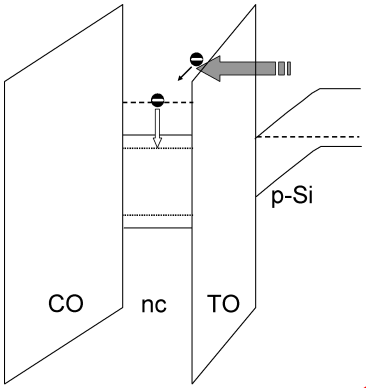
✓ Larger variety of materials using the same deposition method

✓ More suitable material due the wide range on $E_F$ to select.

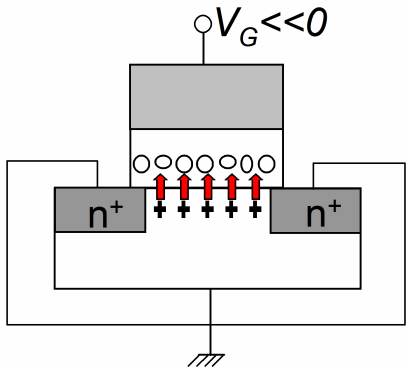
# Introduction to NP Memories: Principle of operation

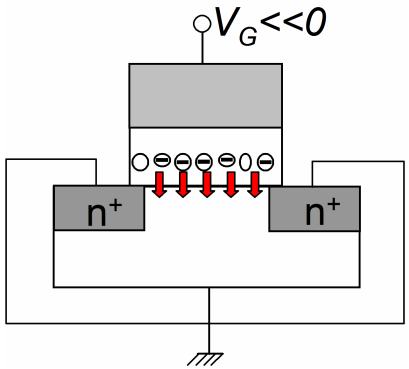
## F-N "Write"

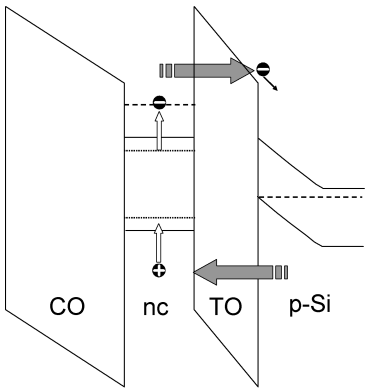


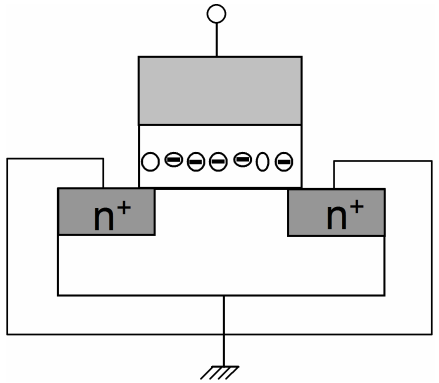

## F-N "Erase"

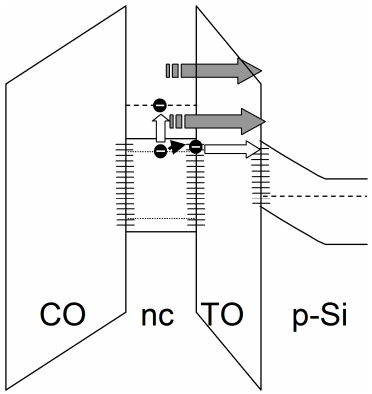


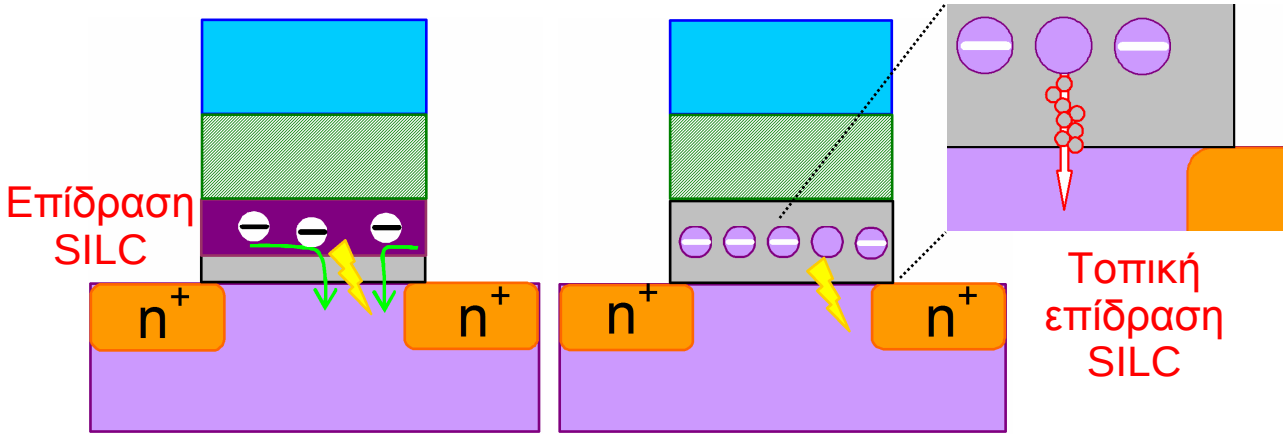

## "Retention mode"



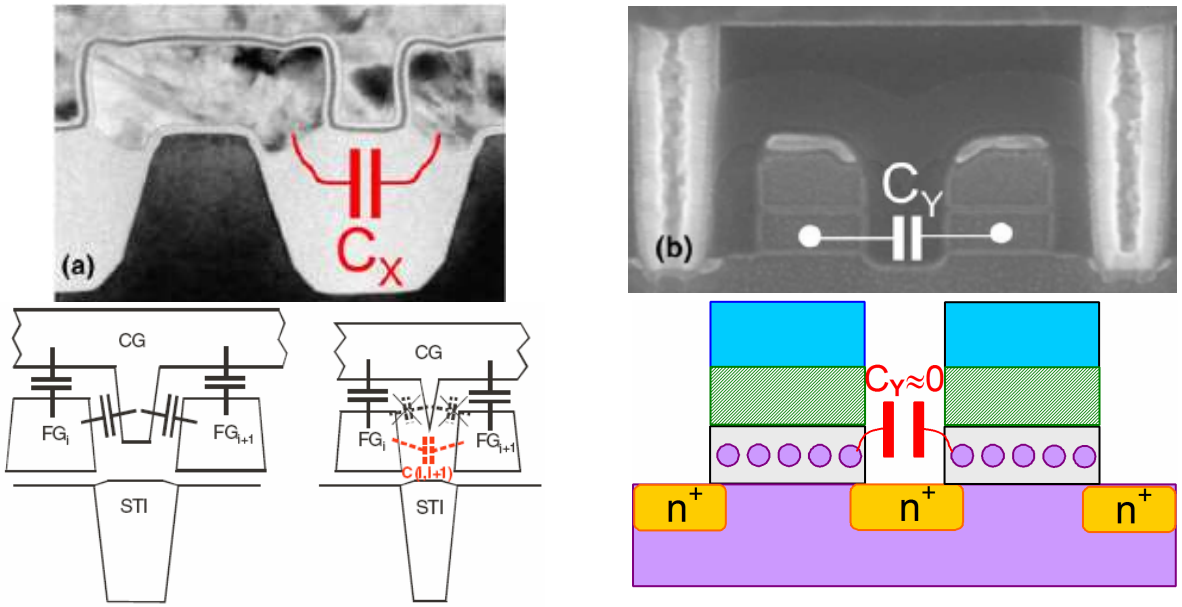



# Advantages of NP Memories

1. Reduction of the thickness of tunnel oxide




2. Increase the density of integration




*P.Dimitrakis, Chapter 8 in "Silicon Nanophotonics", ed. L.Khriachtchev, 2008*

# Fabrication methods in CMOS environment

Optimum size of the NCs lies below the current lithography resolution

⇒

Use of self-assembly process

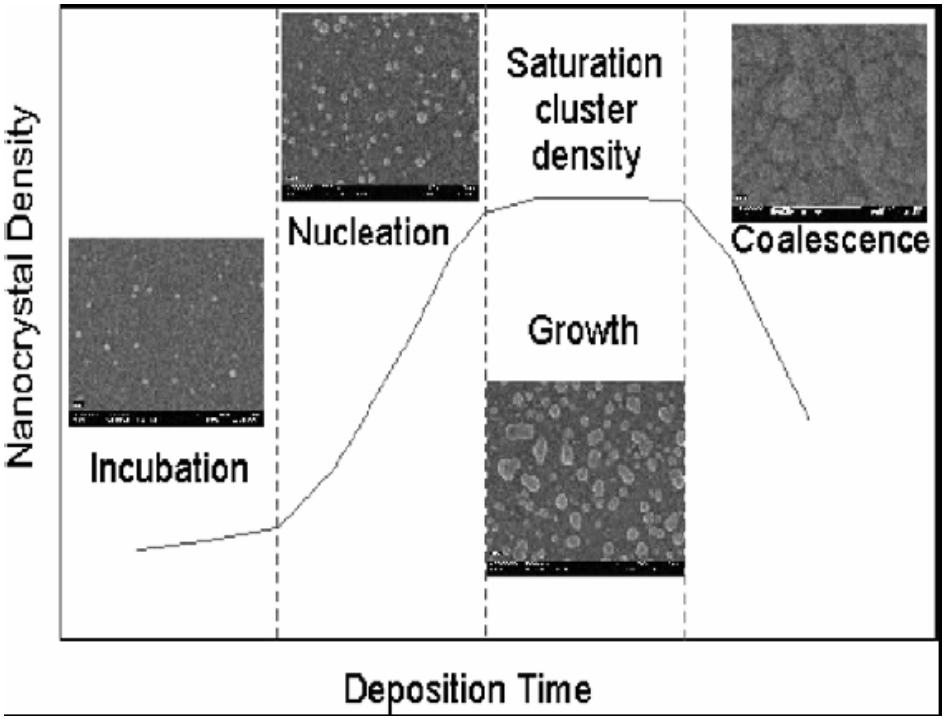
**Deposition**

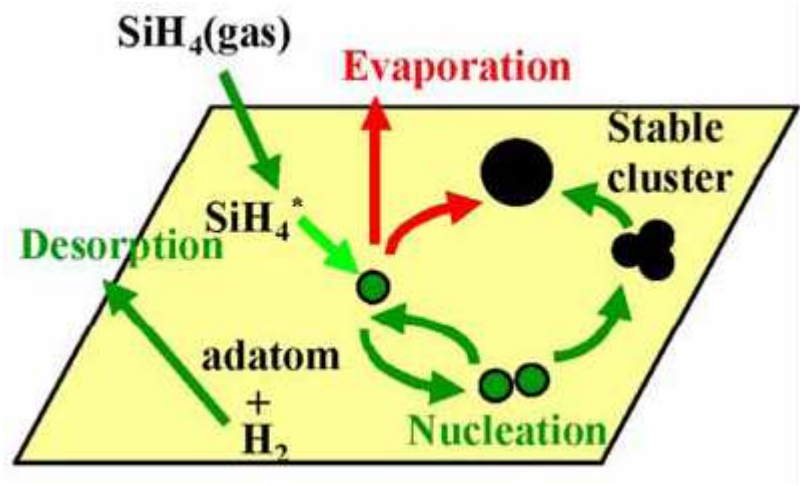
- CVD
- Aerosol
- Magnetron Sputtering
- MBE…..

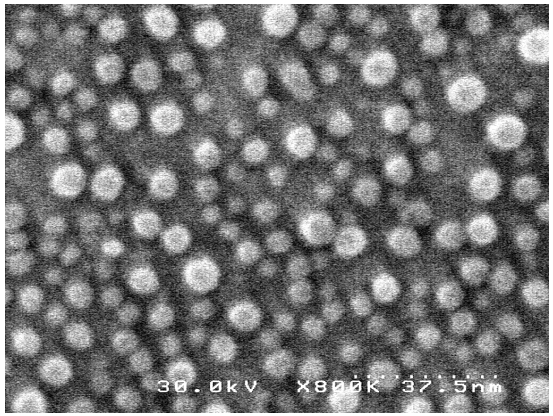
**Thermal Oxidation of a-Si, $Si_{1-x}Ge_x$ , …**

**Ion Beam Synthesis**

# Fabrication methods : LPCVD




$$Ns \sim R^{2i/5} \exp\left(\frac{2}{3}\frac{E_i + (i+1)E_a - E_d}{kT}\right)$$

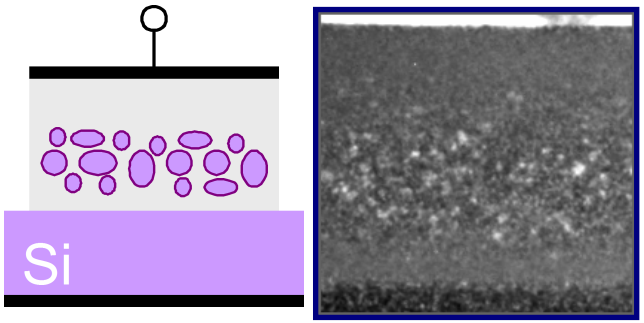
Density: ~$9.6\times10^{11}$cm$^{-2}$

<Diameter>: ~5nm

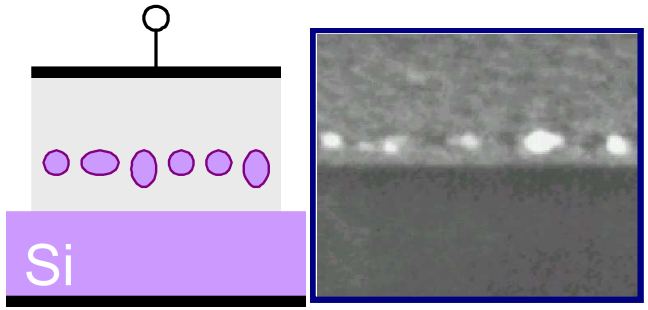
# Fabrication methods : ULE-IBS

Main advantages of ULE-IBS

- ✓ 2-D array of Si NPs.
- ✓ Small variation of NP's size



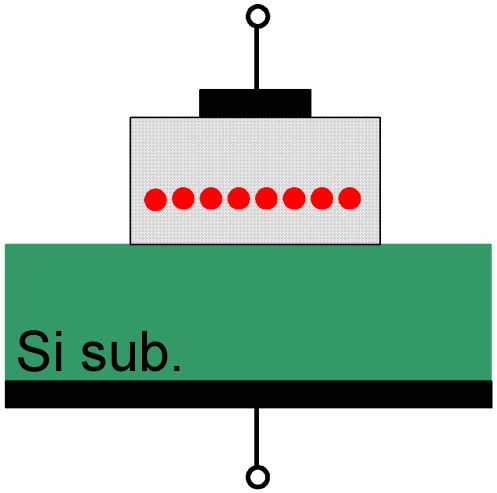

High energy implantation

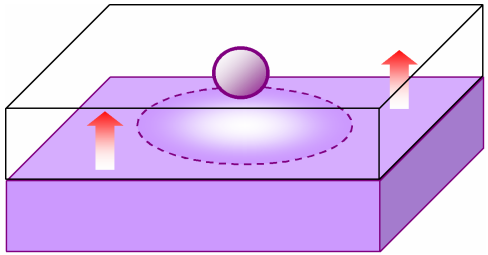


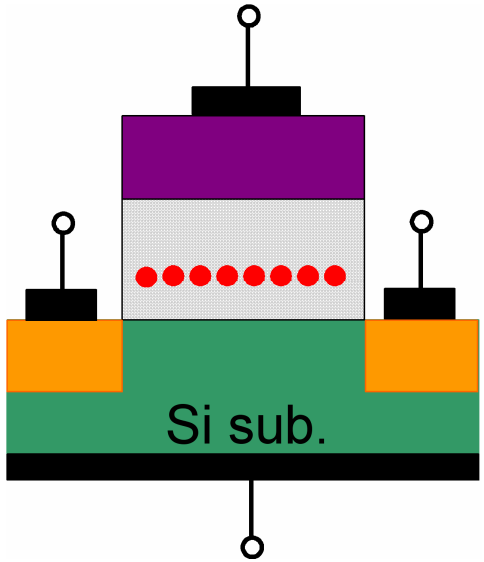

Low energy implantation

# Test structures

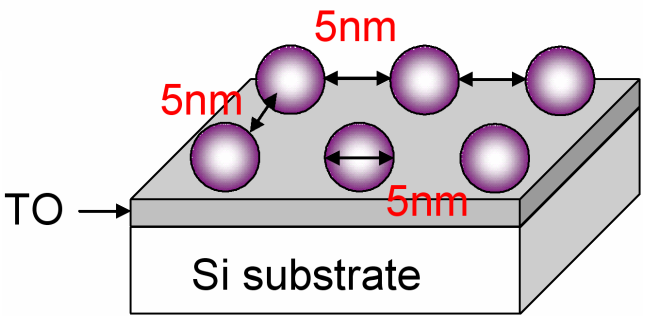
- MIS capacitors
  - C-V vs test signal *f*
  - Quasi-static C-V
  - I-V vs sweep/ramp rates
  - Electrons or Holes?
- MISFET
  - Threshold voltage calculation
  - Transfer characteristics ($I_{DS}$-$V_{GS}$)
  - Output characteristics ($I_{DS}$-$V_{DS}$)
  - Parasitics (leakage current etc)





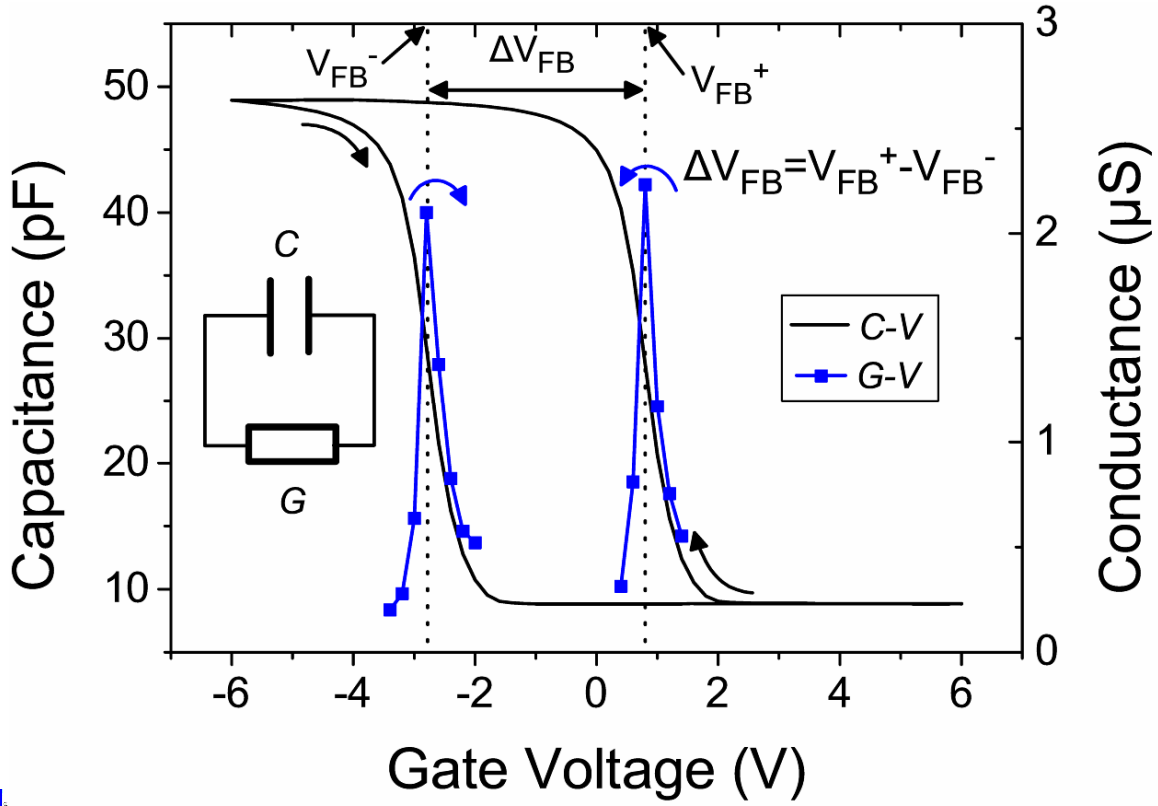

nc 2-D array



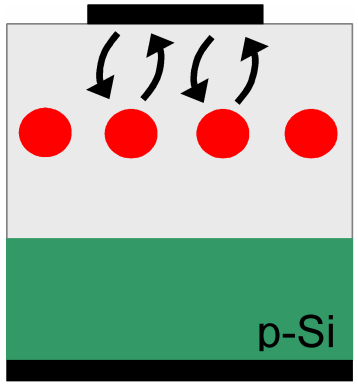
# Memory Window Definition

- MIS capacitors
  - $\Delta V_{fb} = V_{fbP} - V_{fbE}$

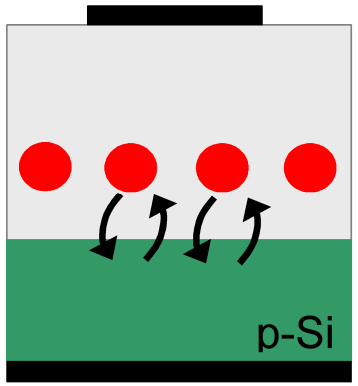
    Calculated after forward and backward voltage sweep or P/E pulses




Counter clockwise hysteresis

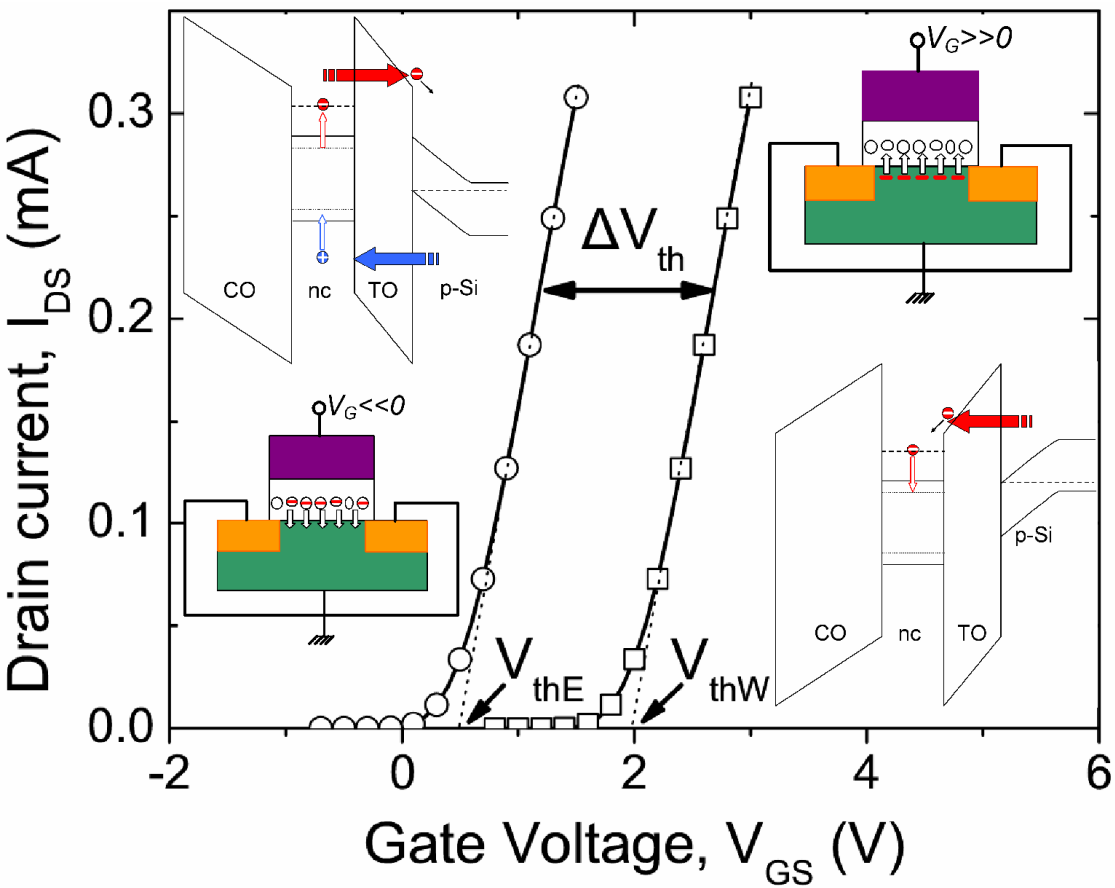



Clockwise hysteresis



# Memory Window Definition

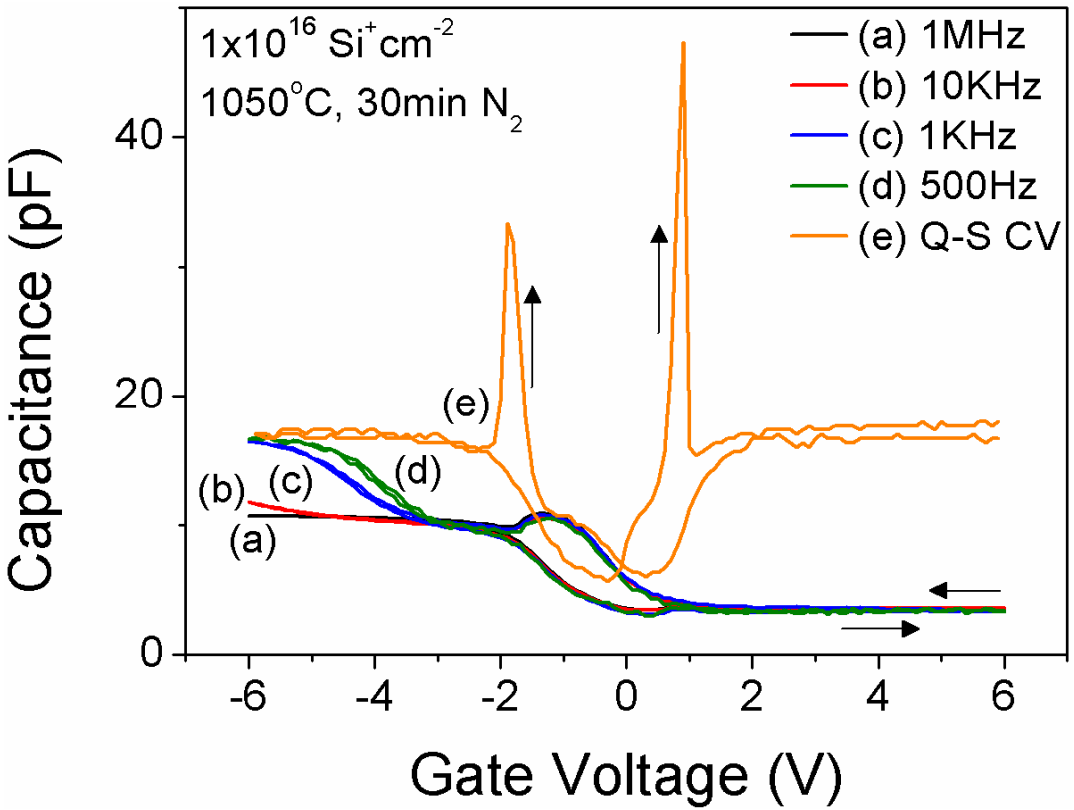
- MISFET
  - $-\Delta V_{th} = V_{thP} - V_{thE}$
  - Calculated after applying P/E voltage pulses

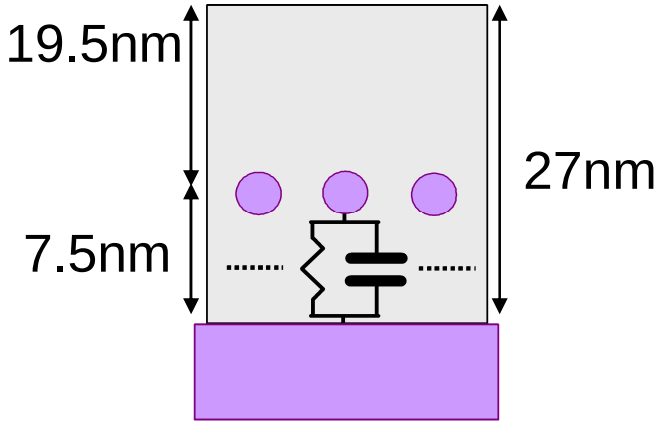



| | PGM | ERS |
|---|---|---|
| NAND | F-N | F-N |
| NOR | DCHE | F-N |

# MISC C-V measurements: Test Signal Frequency effects

- Substrate screening
  - High NC density
  - High TO transparency

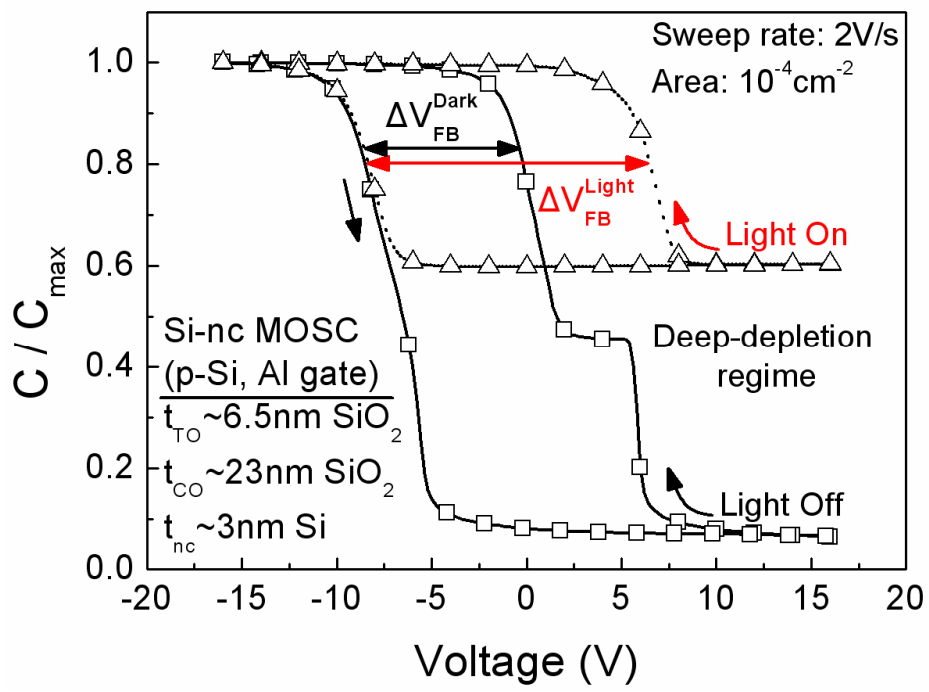


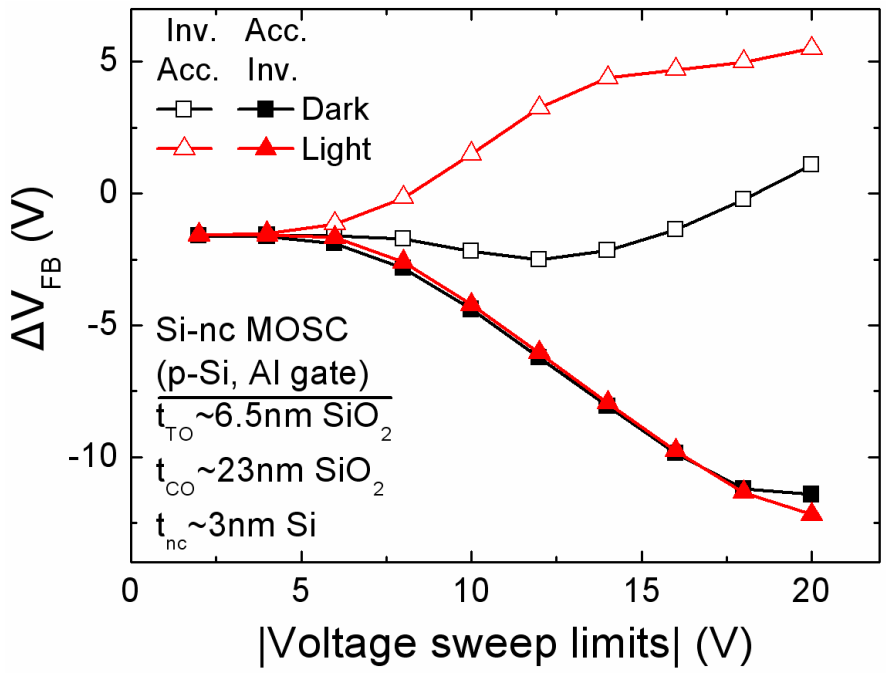




*P.Dimitrakis, MSE B, 2003*

# MISC C-V measurements: Substrate effects

- Tunneling of minority carriers is affected by light illumination

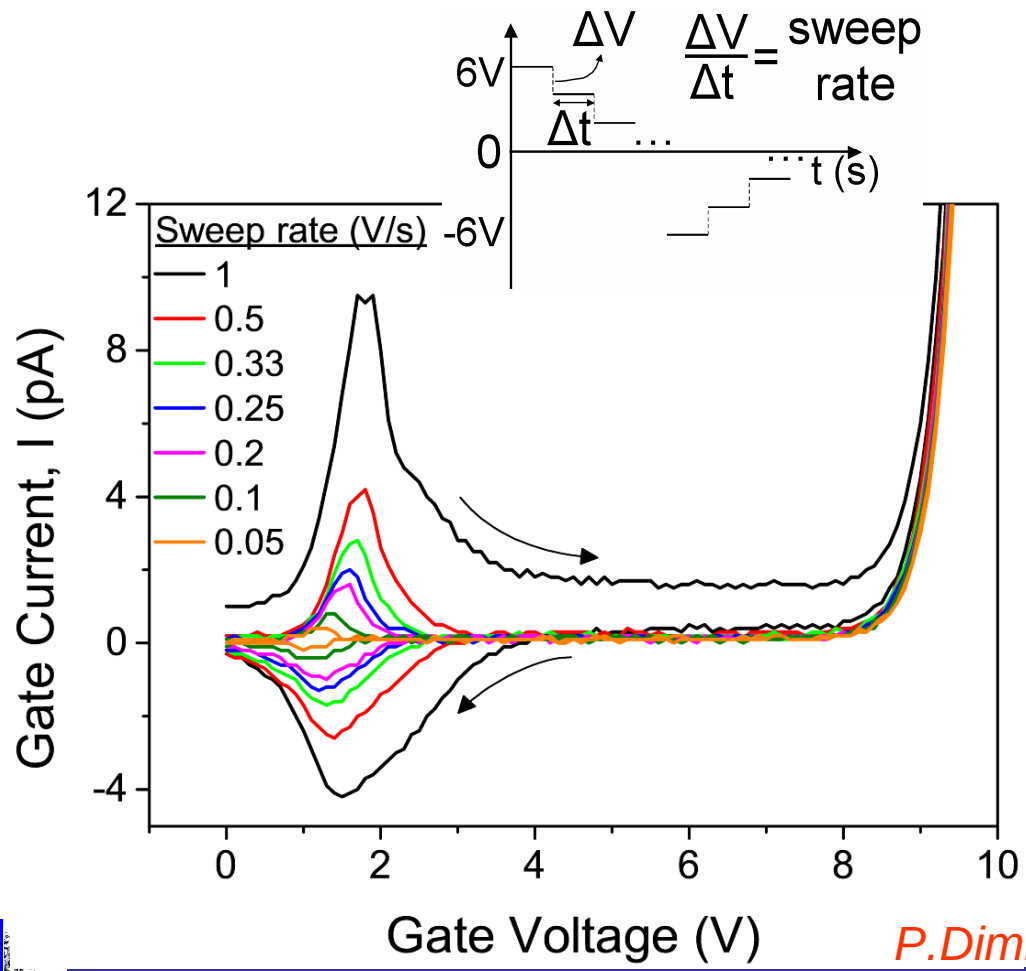


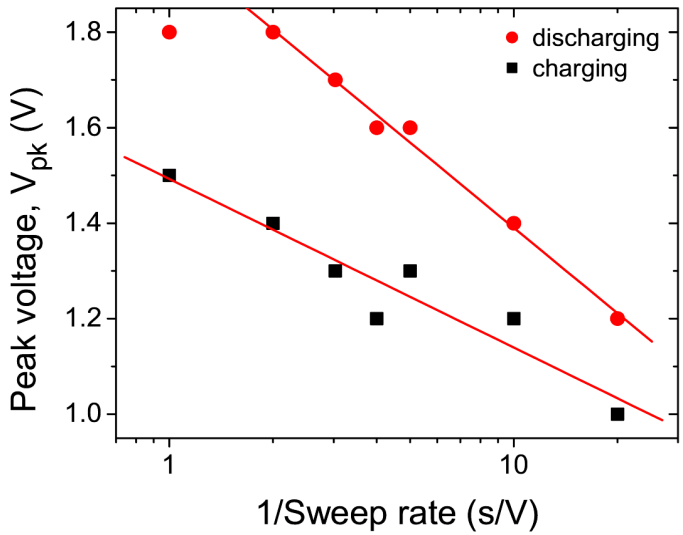



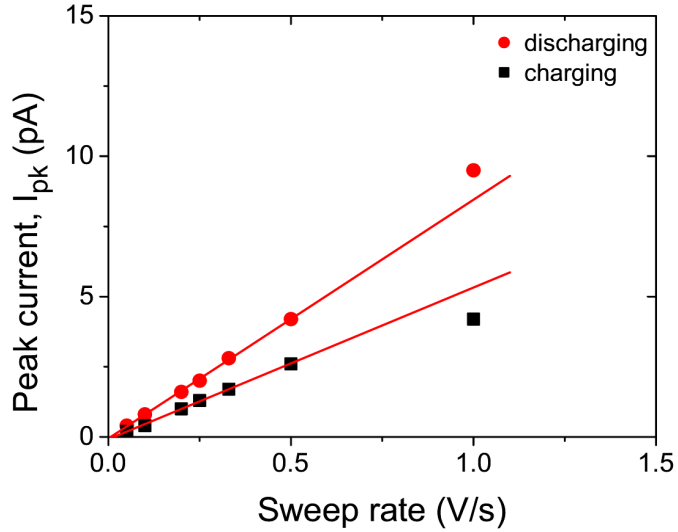

*P.Dimitrakis, Chapter 8 in "Silicon Nanophotonics", ed. L.Khriachtchev, 2008*

# MISC I-V measurements: Sweep rate effects

- Dynamic charging/discharging



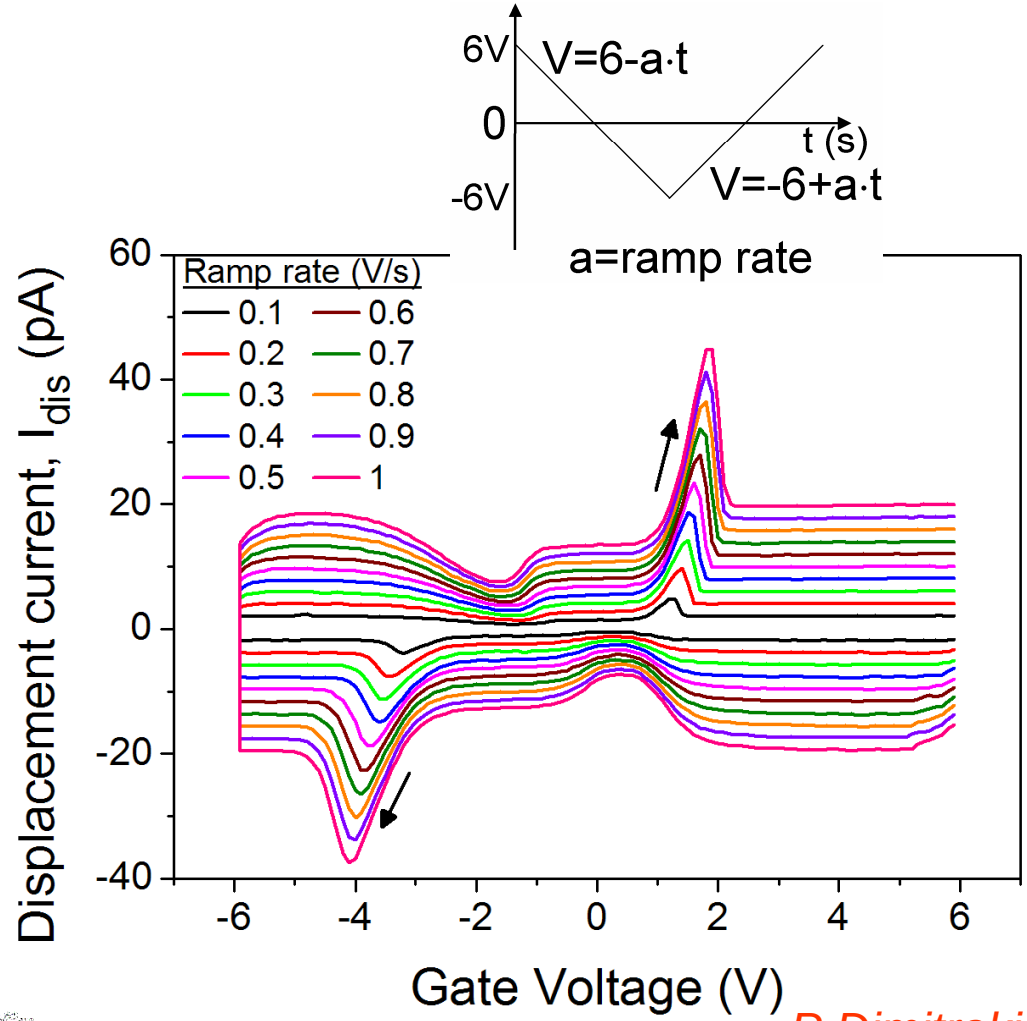



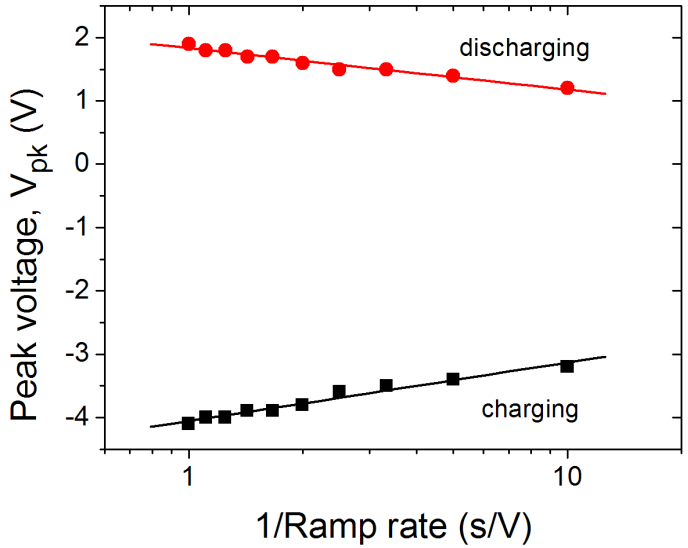



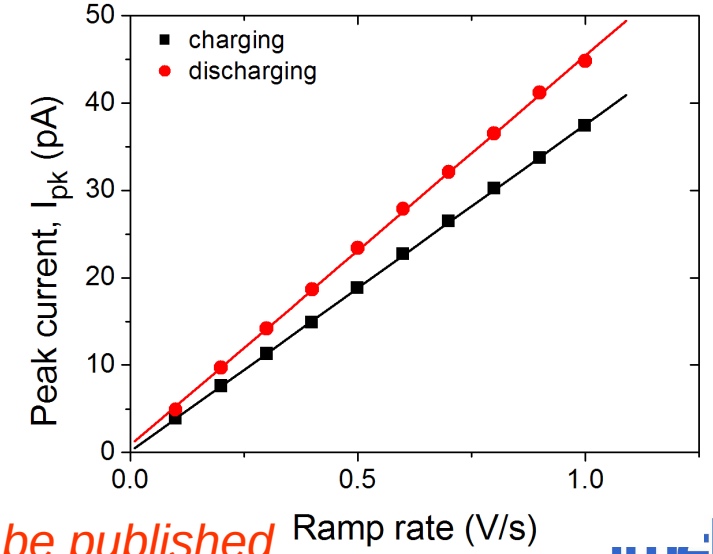

*P.Dimitrakis, to be published*

# MISC I-V measurements: Ramp rate effects

- Charging/Discharging tunneling rate



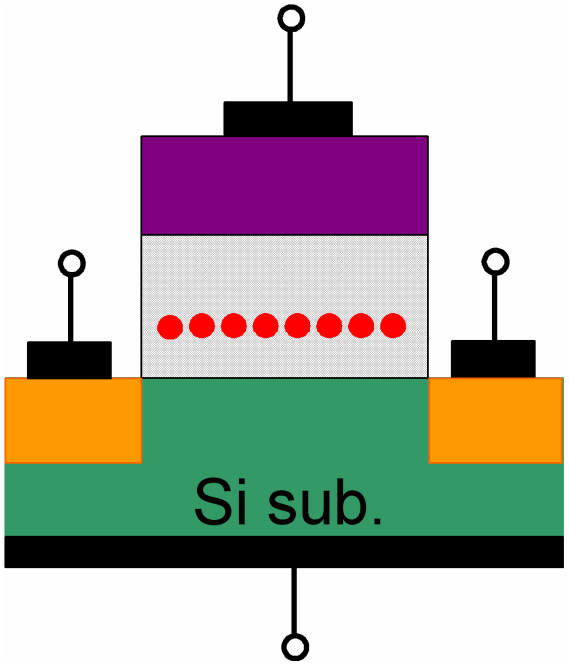




*P.Dimitrakis, to be published*

# NP-MOSFET as Single Memory Cell

**1Bit/T**
2Bit/T
MLC




**IEEE 1005-1998** (Revision of IEEE Std 1005-1991)
**"IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays"**

# MISFET: Threshold voltage definition

- Using linear projection, $g_{m,max}$ etc

  *A. Ortiz-Conde et al. Microelectronics Reliability 42 (2002) 583–596*

- Constant current (CC) method

$$I_{DS}(_{Vth})=I_o\times(W/L)$$

where $I_o=\mu_n C_i K\varphi_t/(8\varphi_F/\varphi_t)^{1/2}\cong$50-100nA for Si channel MISFET

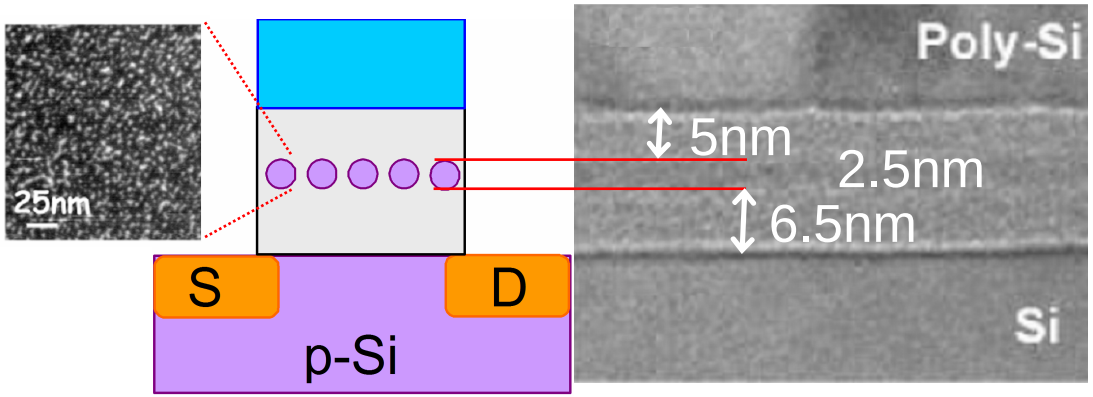
W and L are the gate width and length respectively

$C_i$ gate insulator capacitance

$\mu_n$ electron mobility

# MISFET: P/E characteristics (1)

## First ULE-II Laboratory prototype

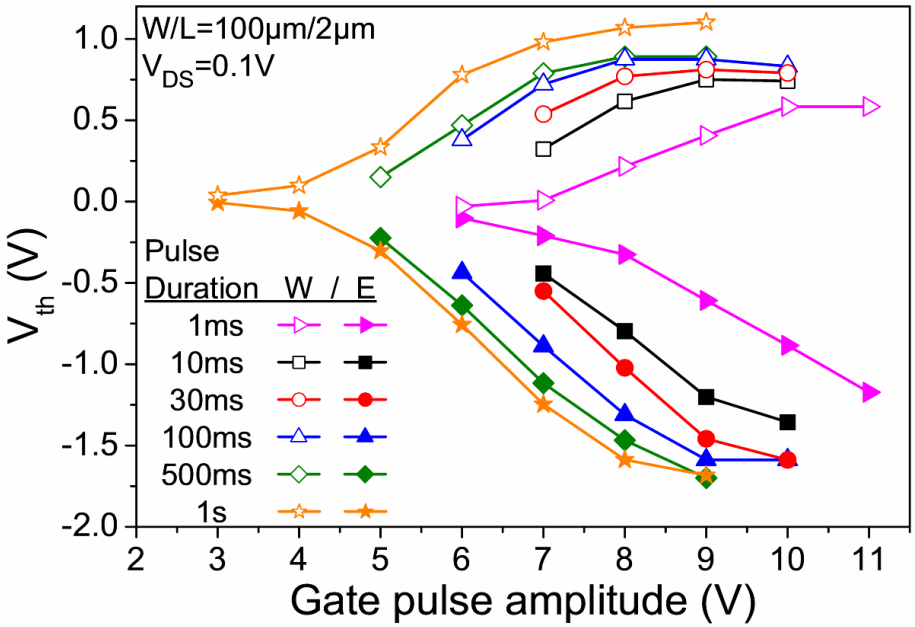



*P.Dimitrakis et al, ESSDERC 2003*

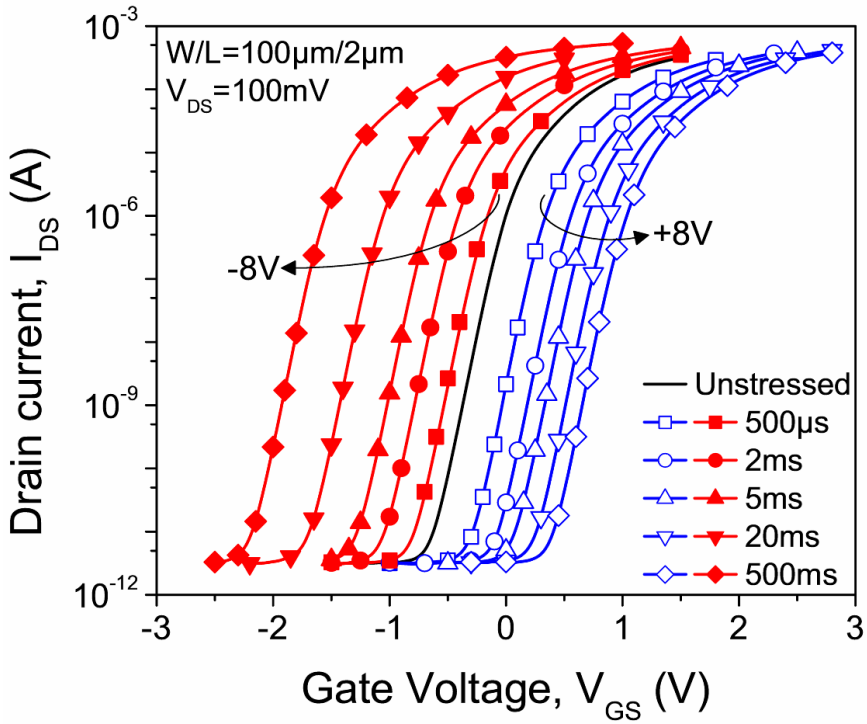
- Fabrication Technology: CMOS 2μm IMEL/NCSR "D"
- ULE-II Technology: Axcelis, USA (1keV/1.5x10$^{16}$ cm$^{-3}$)

# MISFET: P/E characteristics (2)

Constant pulse duration



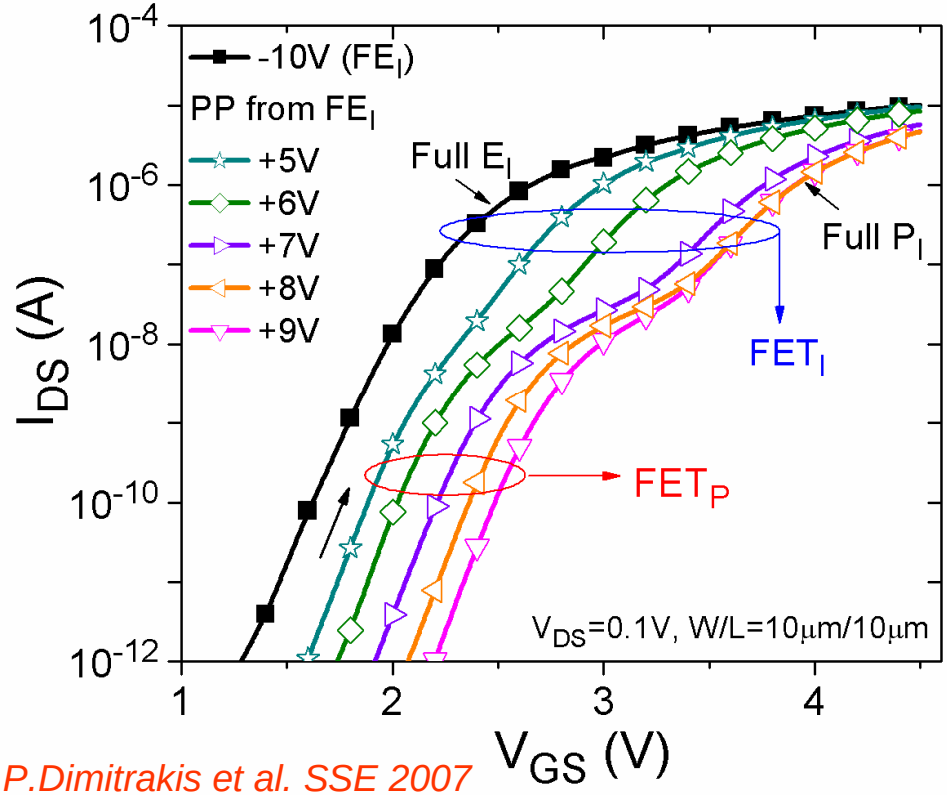

Constant pulse height



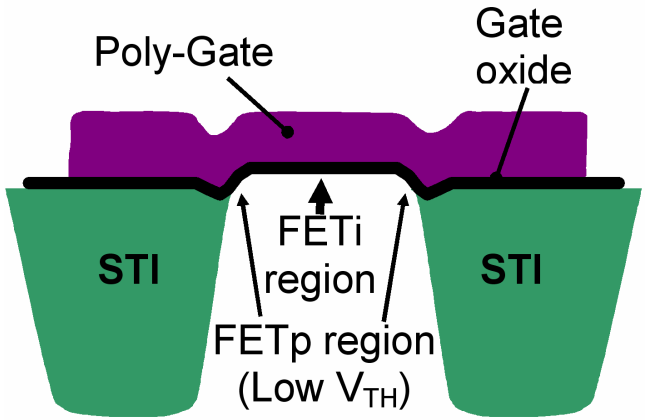

$S$=0.115mV/dec (0.085) $D_{it}$~$5\times10^{11}eV^{-1}cm^{-2}$ $g_{m,max}$=0.28mA/V

*P.Dimitrakis et al. SSE 2004*

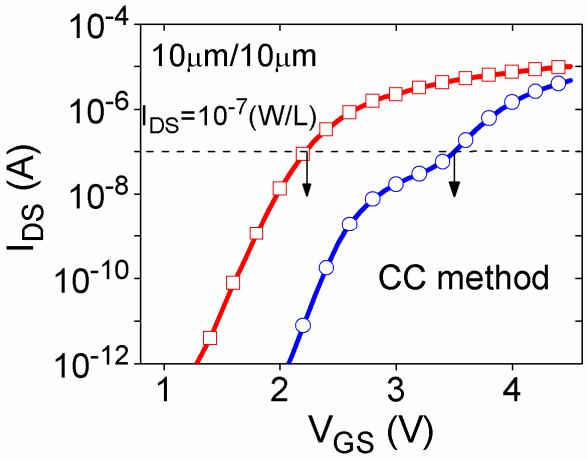
# MISFET: Parasitic transistor (1)



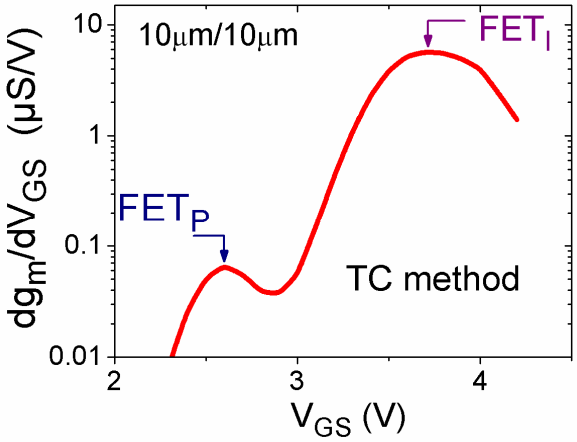

*P.Dimitrakis et al. SSE 2007*




- Constant current method

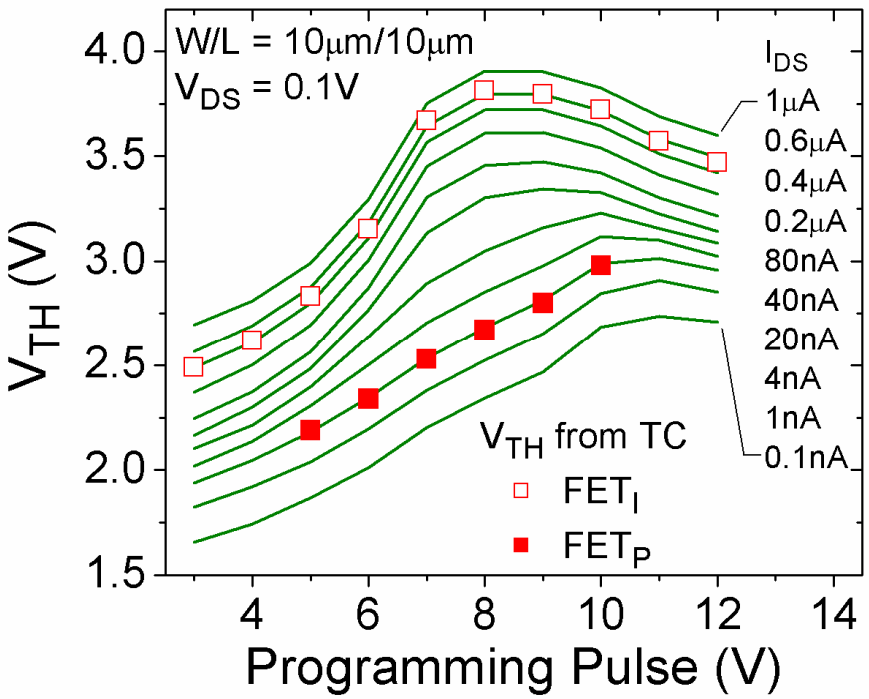



- Transconductance change (TC) method



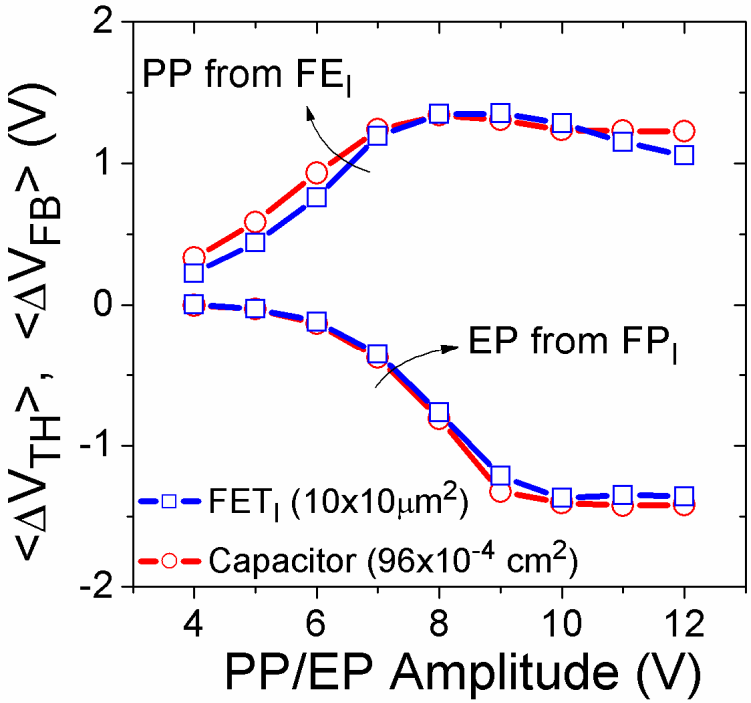
# MISFET: Parasitic Memory Transistor (2)

- Constant current method vs TC method




*P.Dimitrakis et al. SSE 2007*

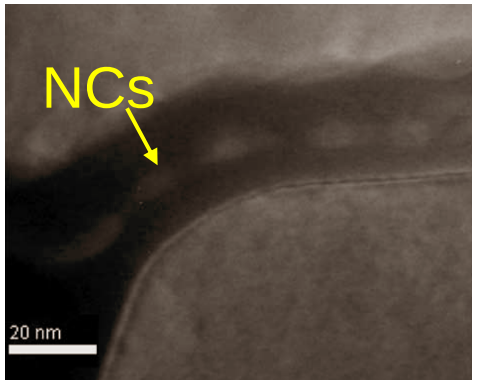
- Constant current method vs TC method

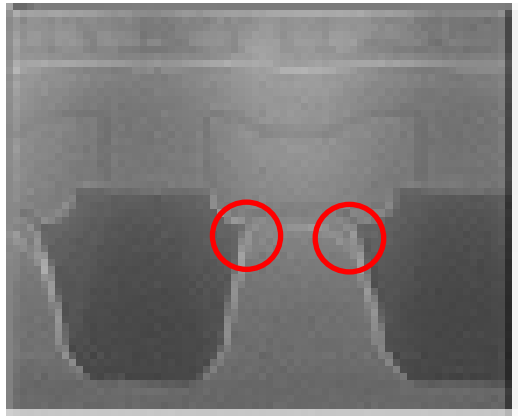


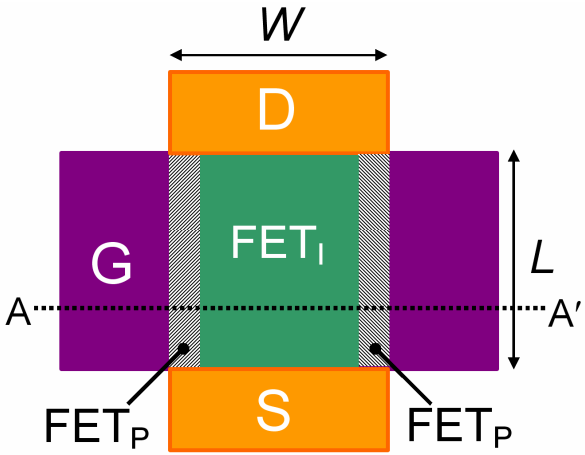

*P.Dimitrakis et al. SSE 2004*

# MISFET: Parasitic Memory Transistor (3)

- Evidence for the existence of PMT

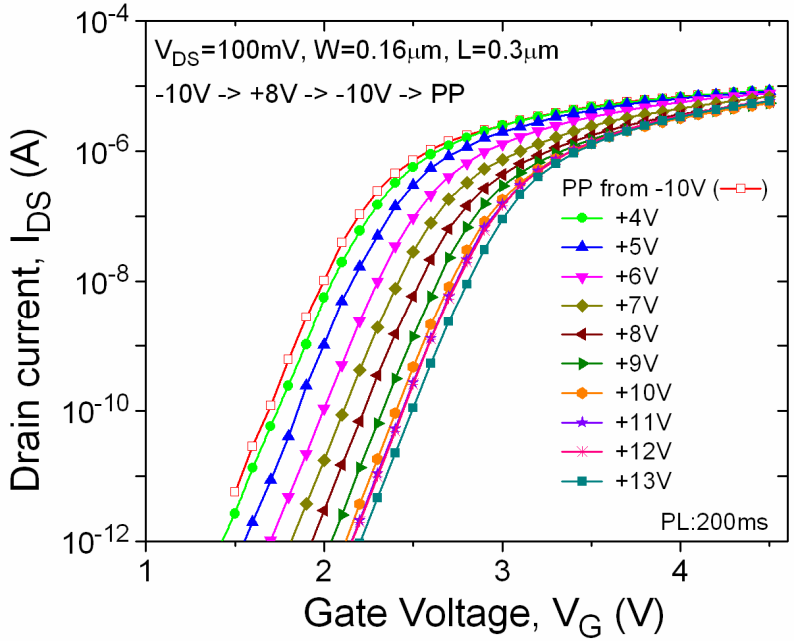


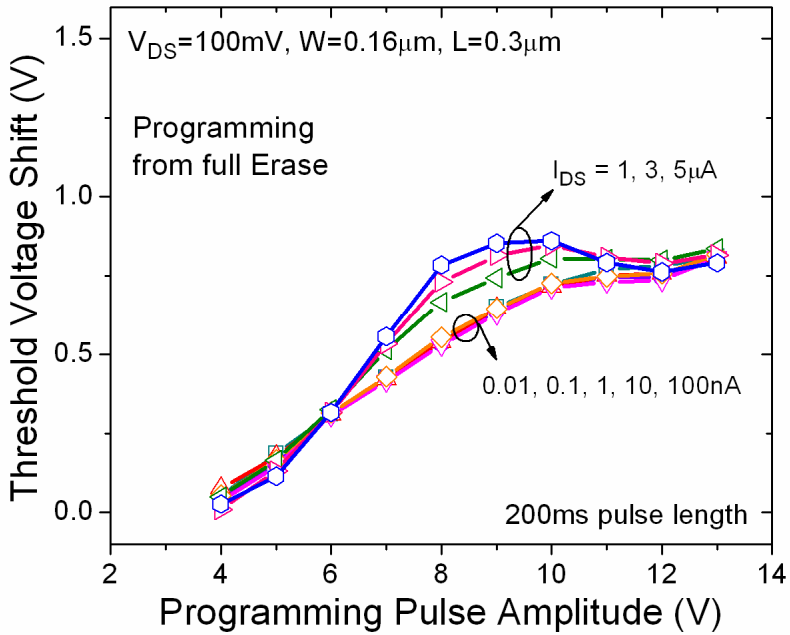






*C.Gerardi, IEEE TED 2007*

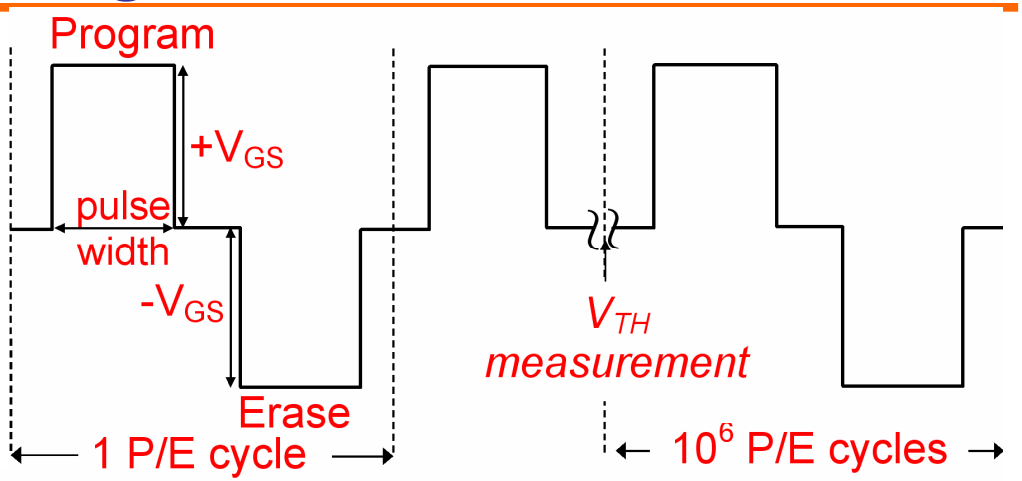
- PMT governs the memory action in deep submicron cells

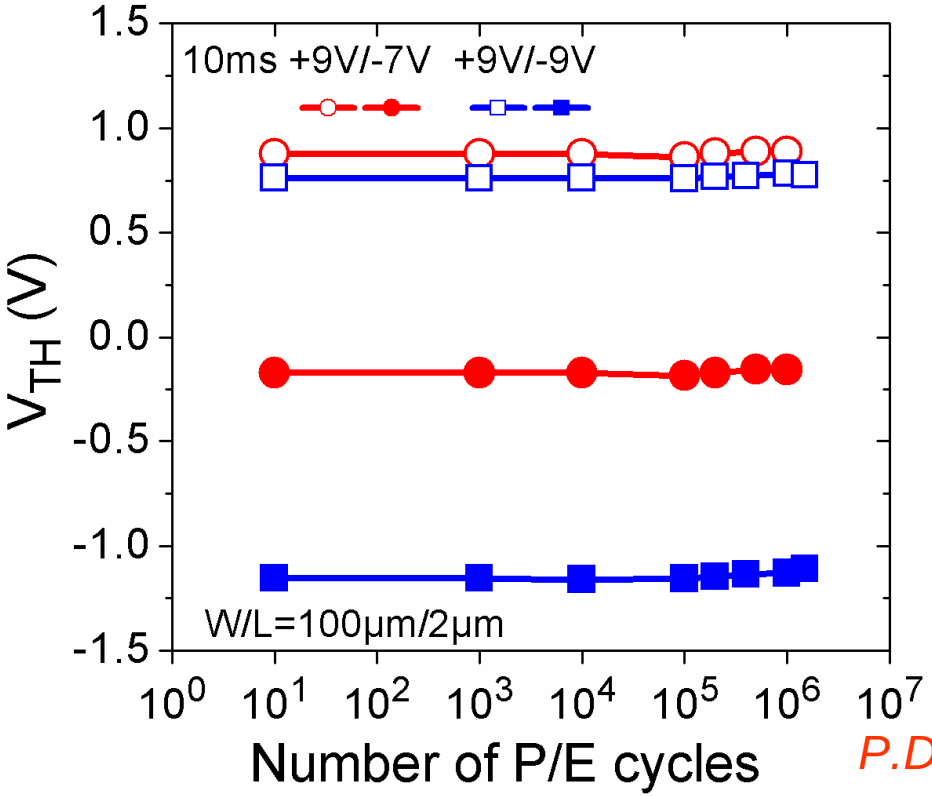


# MISFET: P/E cycling (Endurance test)

- Procedure parameters
  - RT operation
  - Pattern generator
  - Duty cycle effects



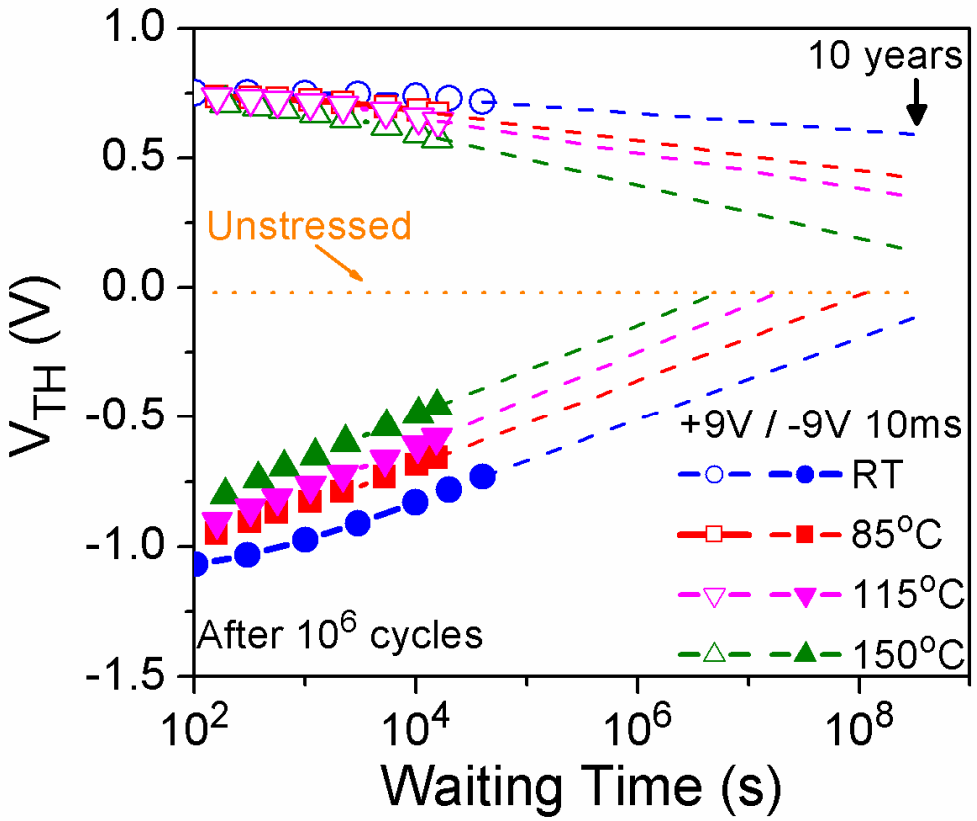




- Neither degradation nor drift in memory window after > $10^6$ 10ms +9V/-9V cycles

*P.Dimitrakis et al. SSE 2004*

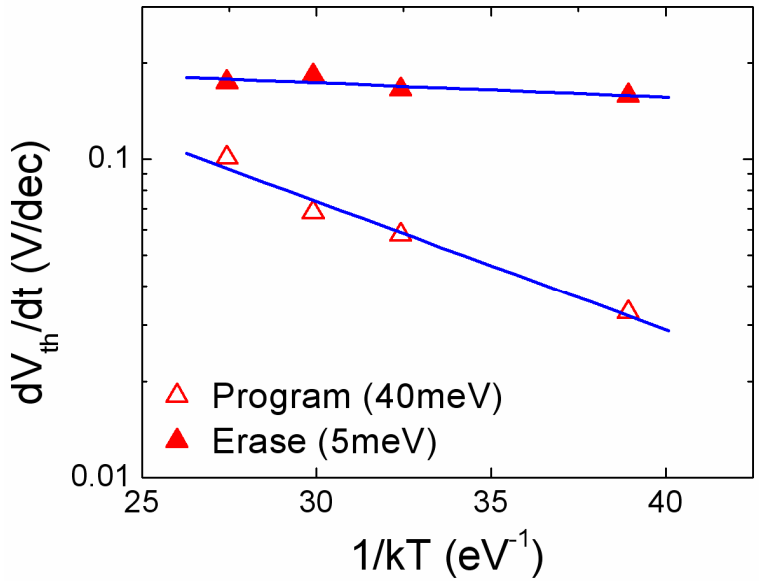
# MISFET: Data retention (1)

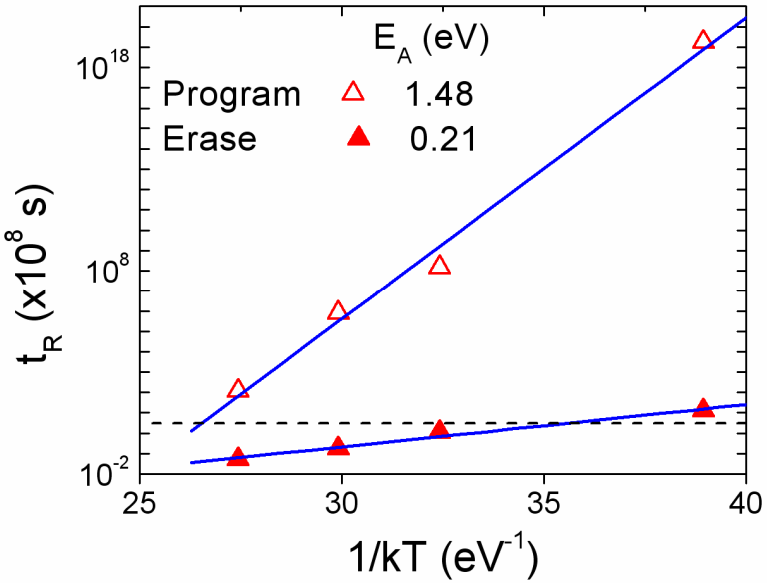
- High temperature accelerates data loss




*P.Dimitrakis et al. SSE 2004*

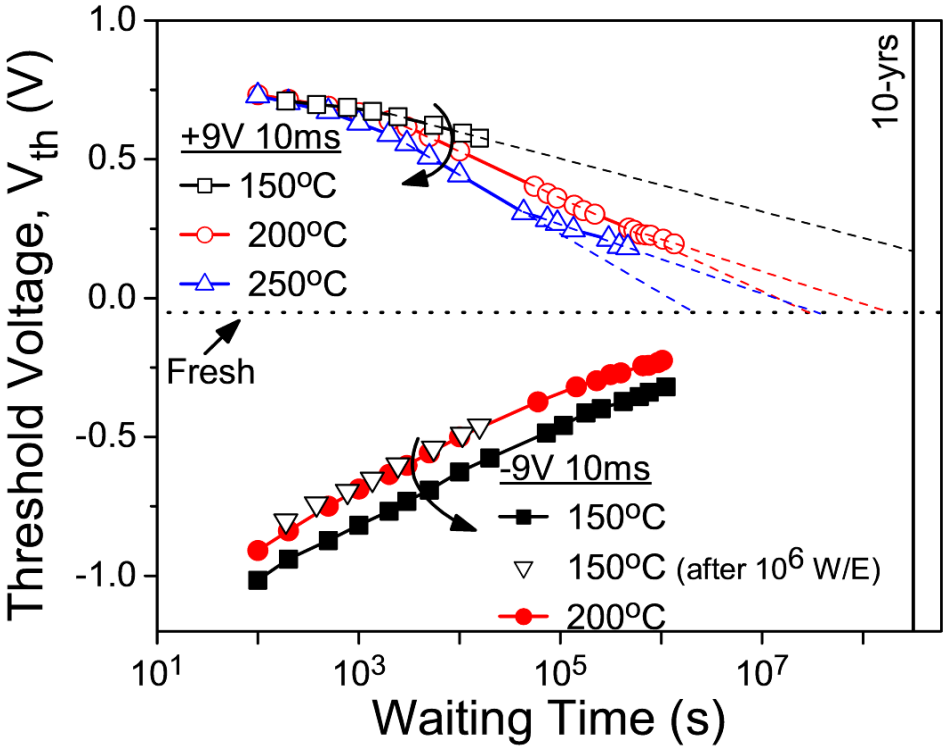
- Investigation of loss mechanisms



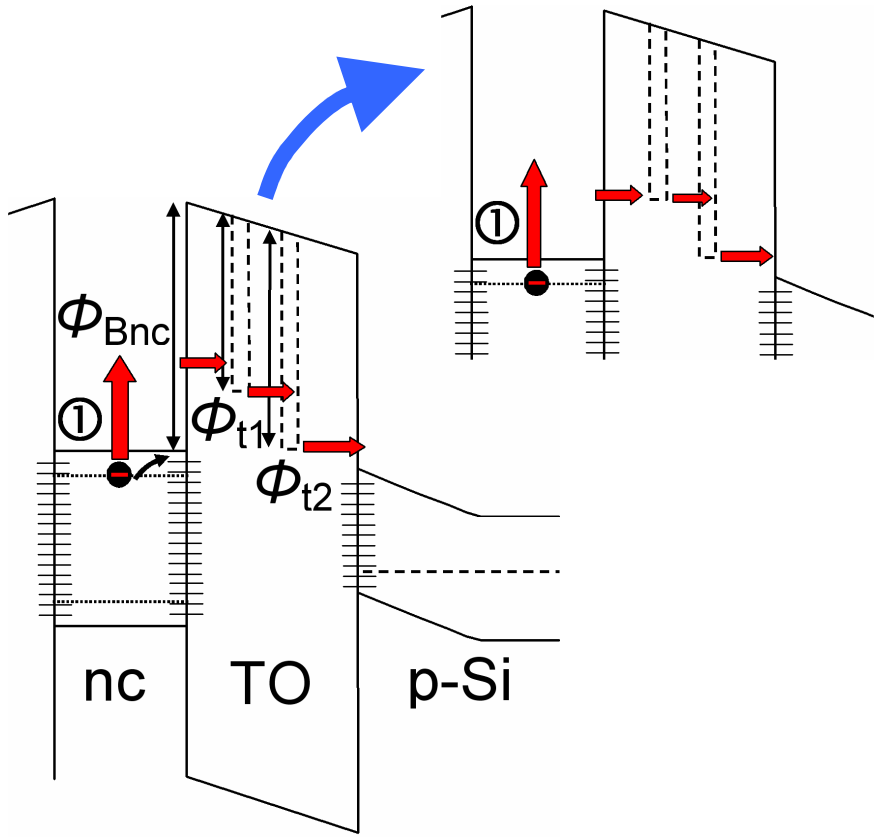
# MISFET: Data retention (2)

- The internal electric field governs the data loss after long time




*P.Dimitrakis et al. MRS Proc. Vol. 830*

Low internal electric field

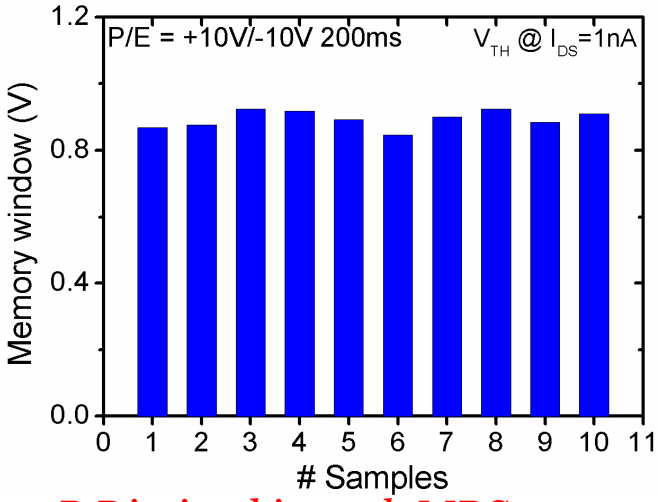



High internal electric field

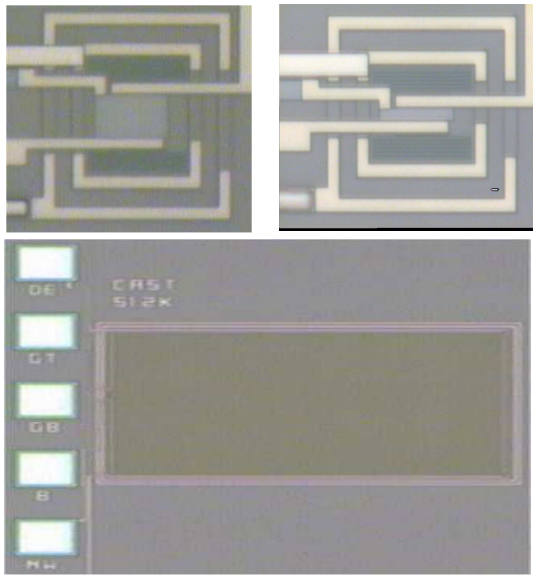
***P.Dimitrakis, Chapter 8 in "Silicon Nanophotonics", ed. L.Khriachtchev, 2008***

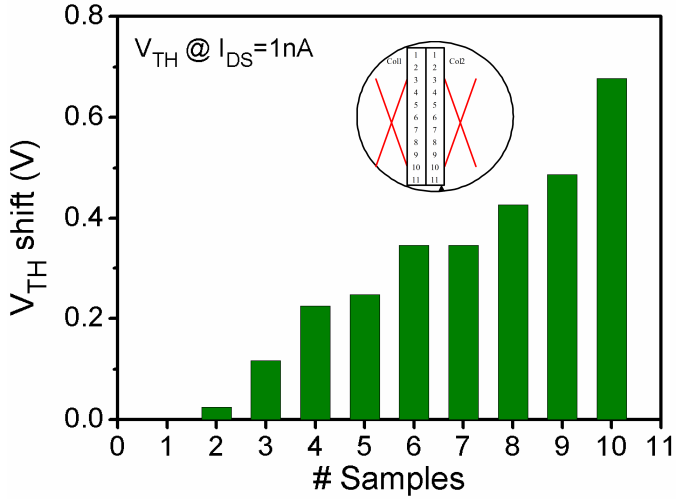
# ULE-II NP Memory cells in a Manufacturing environment

## 200mm p-Si, 0.15μm Double Poly Triple Metal Flash Memory technology




*P.Dimitrakis et al, MRS 2004*



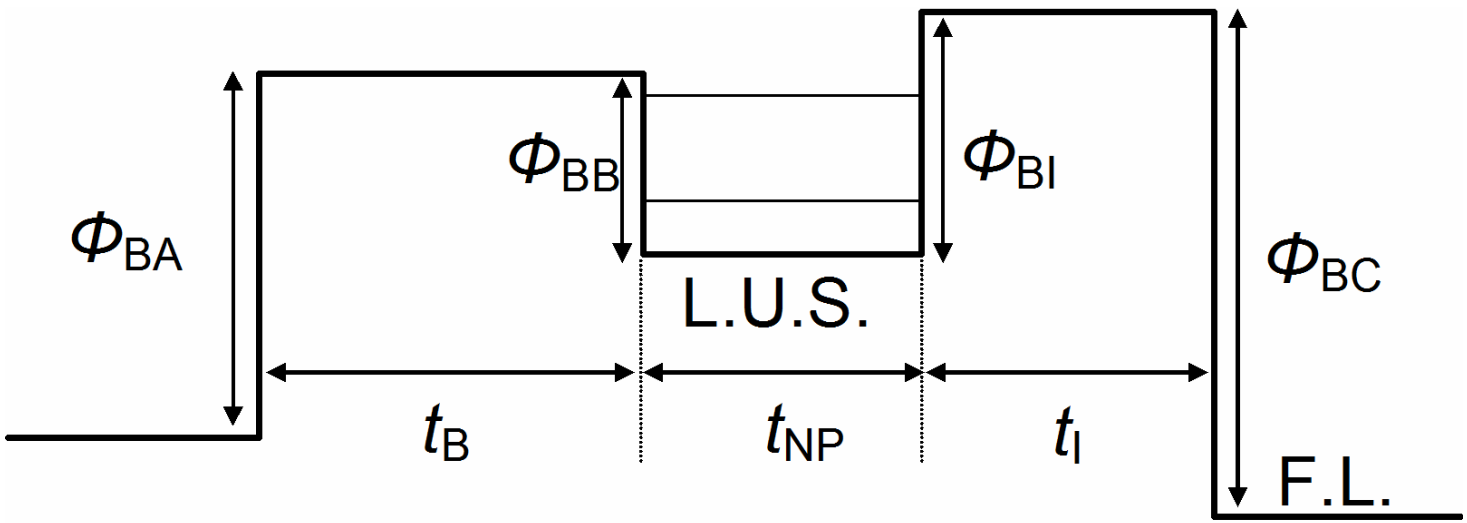



- Uniform memory window across a 200mm Si wafer
  - ✓ ULE-IBS uniform distribution of Si NPs

- Boron contamination causes shift of $V_{th}$ across the Si wafer
  - ✓ A dedicated or "clean" ion implanter is required

# Optimization – New cell architectures (1/9)

- Maximize memory window ($\Delta V_{th}$) ⇒ The tunneling current from Si substrate to NCs should be maximized.
- Maximize endurance (No P/E) ⇒ The SILC effect should be minimized
- Maximize charge retention ⇒ The back tunneling current from NCs to control gate should be minimized.
- Maximize charge retention ⇒ The tunneling-back current from NCs to the Si substrate should be minimized.

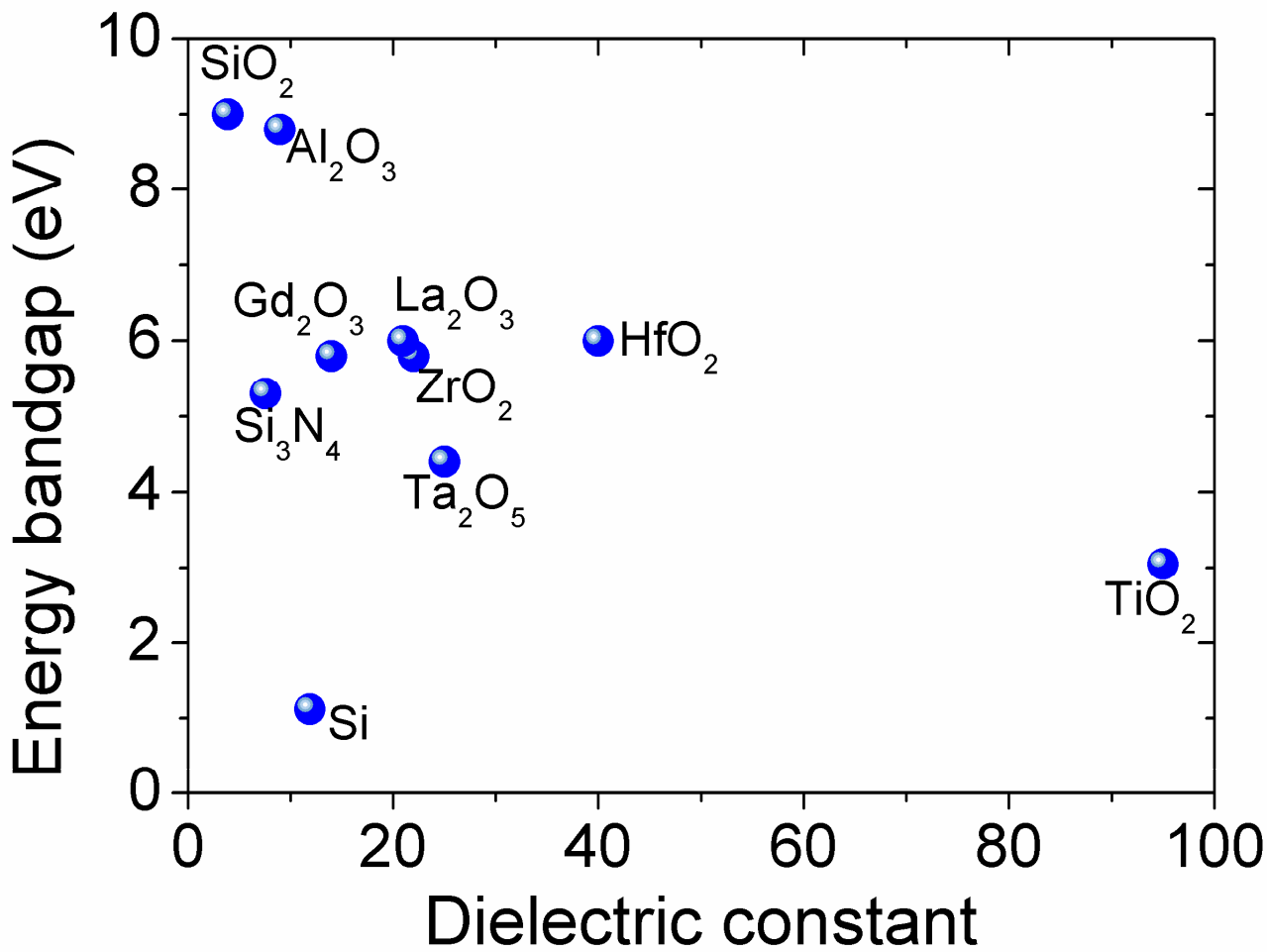


# Optimization – New cell architectures (2/9)

| **Operation** | $\Phi_{BC}$ | $t_I$ | $\Phi_{BI}$ | $\Phi_{BB}$ | $t_B$ | $\Phi_{BA}$ |
|---|---|---|---|---|---|---|
| **Write** (Low V & fast) | $<\Phi_{BI}$ | ↓ | $>\Phi_{BC}$ & $\leq\Phi_{BB}$ | $>\Phi_{BA}$ & $\geq\Phi_{BI}$ | $E_B<E_I$ | $<\Phi_{BB}$ |
| **Erase** (Low V & fast) | $>\Phi_{BI}$ | ↓ | $<\Phi_{BC}$ | $<\Phi_{BA}$ | $E_B<E_I$ | $>\Phi_{BB}$ |
| **Retention** (10years @ High-T) | $<\Phi_{BI}$ | ↑ | $>\Phi_{BC}$ & $\geq\Phi_{BB}$ | $>\Phi_{BA}$ | ↑ | $<\Phi_{BB}$ |
| **Read** | Not affected | Not affected | Not affected | Not affected | Not affected | Not affected |
| | Cathode material property | Depends on its conduction properties | Depends on (i) NP's size and (ii) injection & blocking materials | | Depends on its conduction properties | Anode material property |

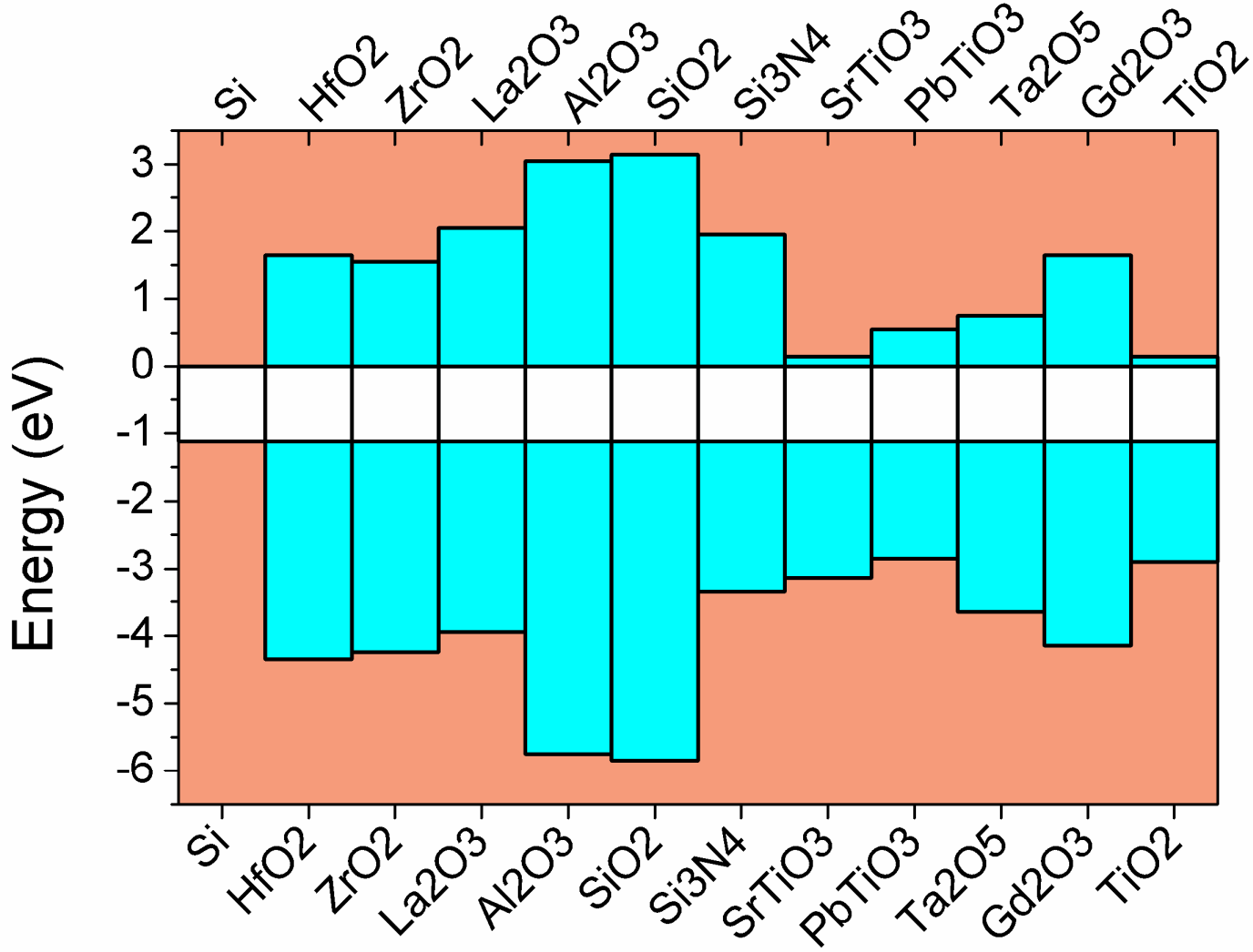
# Optimization – New cell architectures (3/9)

The energy bandgap decreases as the dielectric increases



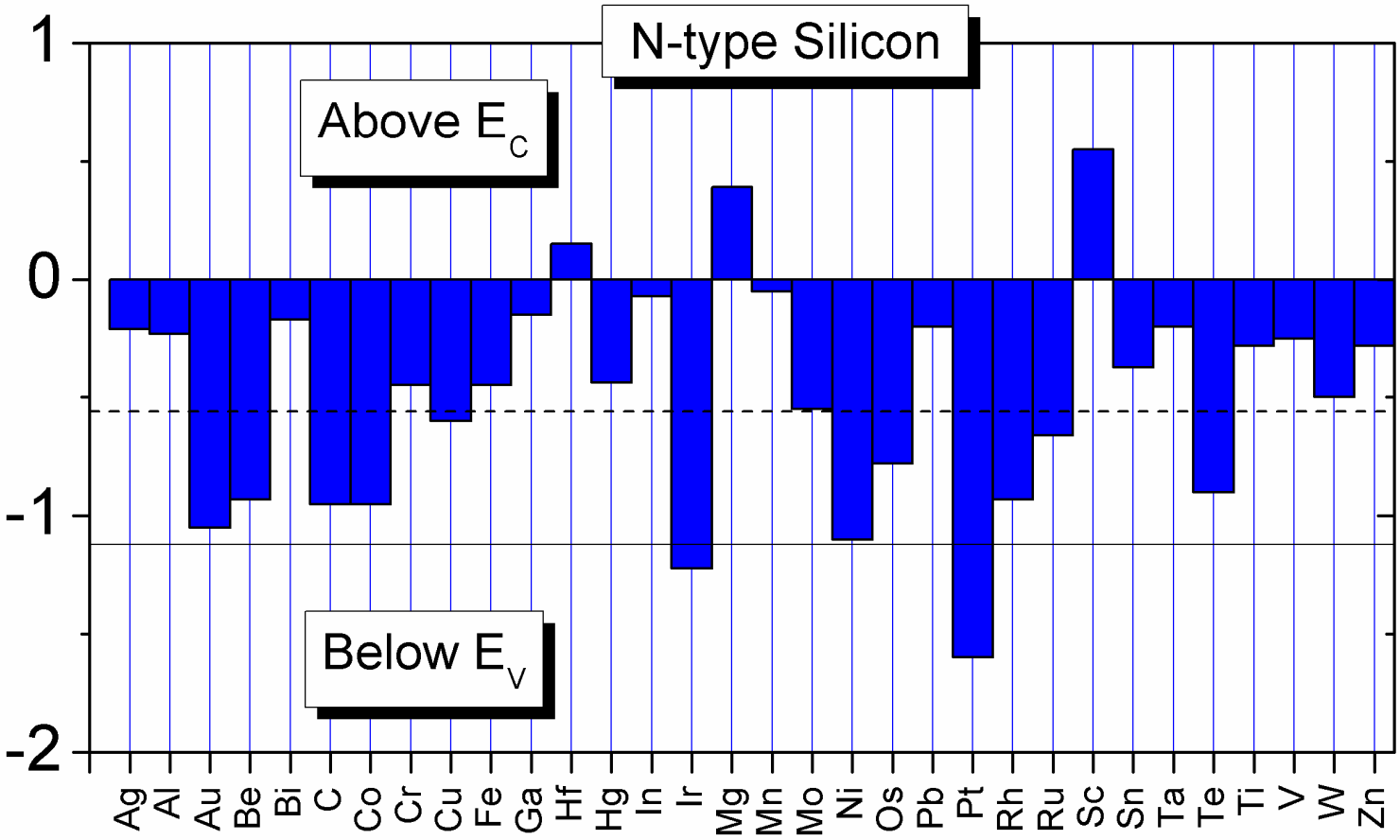
# Optimization – New cell architectures (4/9)

Selection of blocking and injection dielectric materials regarding their conduction band offset with respect to Si



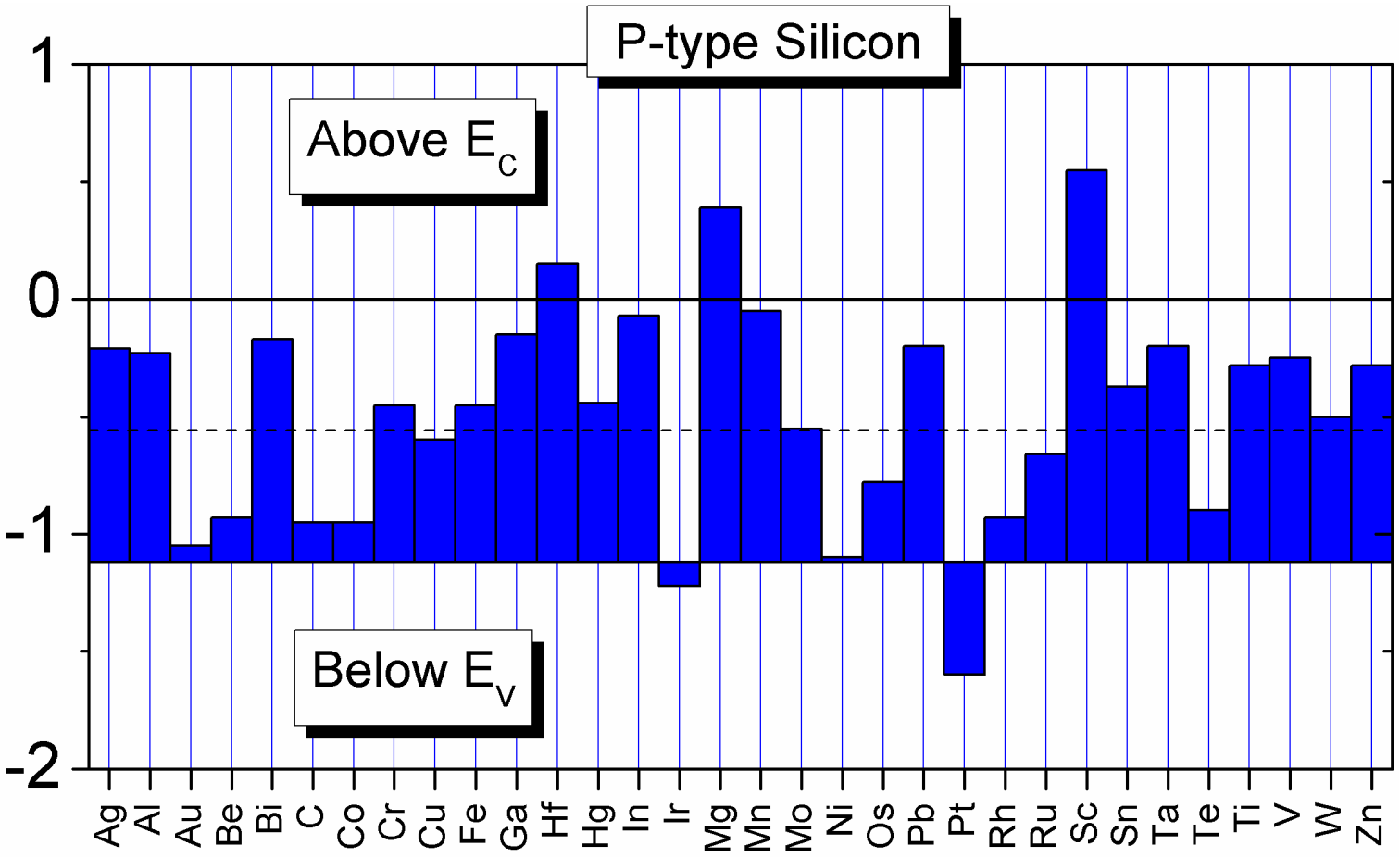
# Optimization – New cell architectures (5/9)

## Selection of NP material regarding their LUS or conduction band offset



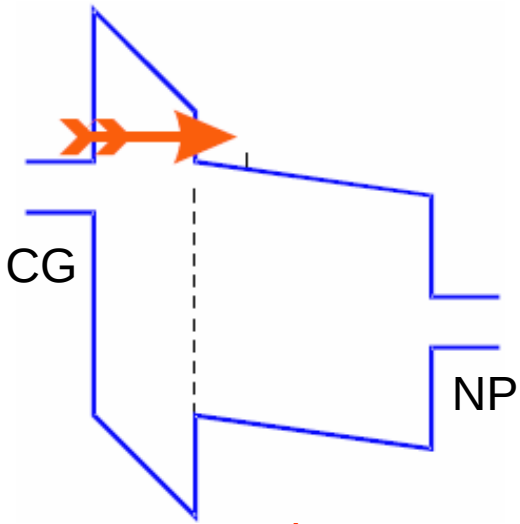
# Optimization – New cell architectures (6/9)

## Selection of NP material regarding their LUS or conduction band offset

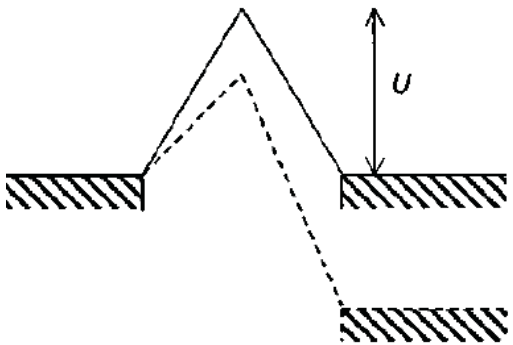


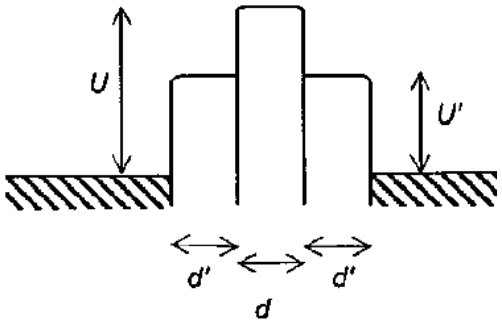
# Optimization – New cell architectures (7/9)

- Blocking and injection dielectrics made of single material layer reduces the degrees of freedom to face the optimization issues ⇒ a multilayer approach is more preferable
- Injection dielectric options
  - VARiable Oxide Thickness (VARIOT) This approach optimizes the current injection using 2 different dielectrics (Lo-Hi-k)
  - Crested barrier This approach optimizes the current injection using 3 different dielectrics (Hi-Lo-Hi-k)




Govoreanu et al., IEEE EDL 24, 99 (2003)



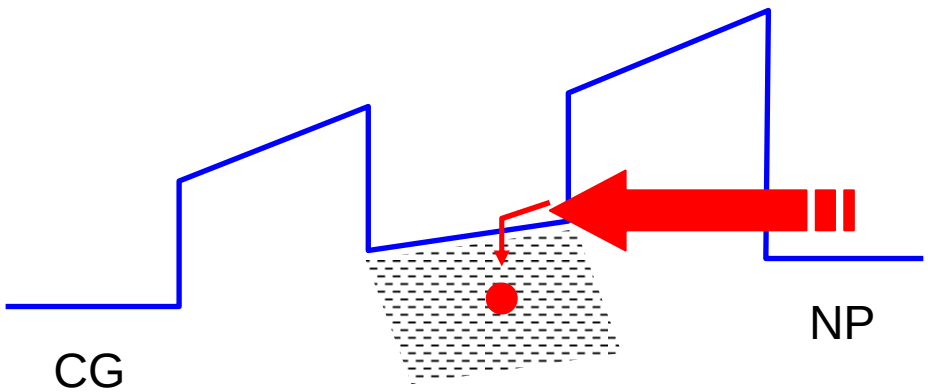

K.Likharev, APL 73, 2137 (1998)

Baik et al., IEDM 2003, Samsung

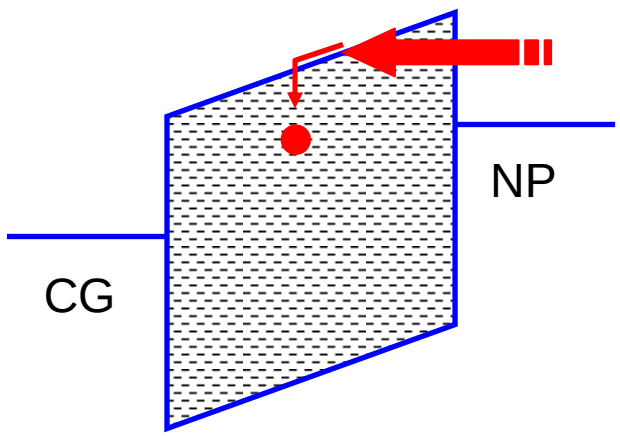
# Optimization – New cell architectures (8/9)

- Blocking dielectric options
  - Lo-Hi-Lo-k Trilayer structure.
  - "Trappy" single high-k layer

  This approach enhance the charge leakage to the gate electrode but care should be taken to avoid electron charging from the gate during ERS



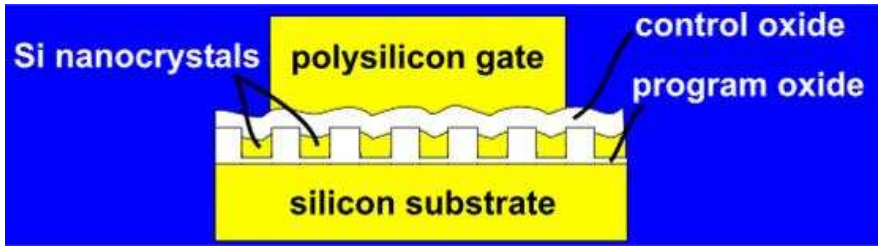

**Lo - Hi - Lo-k**



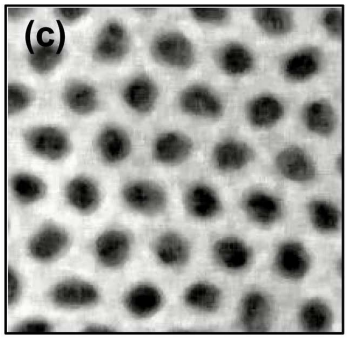

"Trappy" Hi-k

# Optimization – New cell architectures (9/9)

- Uniformity of NPs' size distribution and other geometrical characteristics (surface density, interdot distance etc.)
- Repeatability & large scale integration (variation from batch to batch, 300mm Si wafers etc)
  - NPs through Templates, Stencils, Pattern Transfer etc




Block-Copolymer Self-Assembly Assisted Si-NC Fabrication

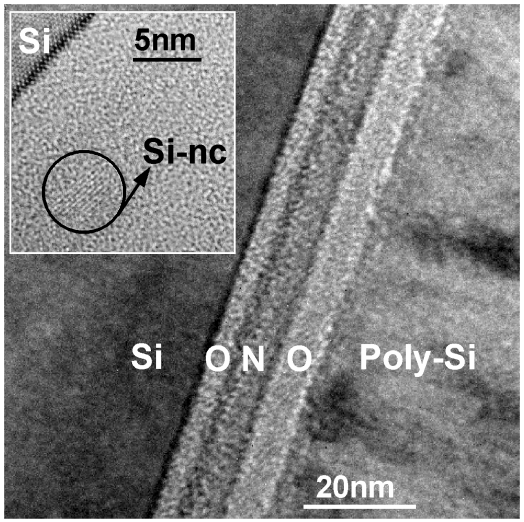


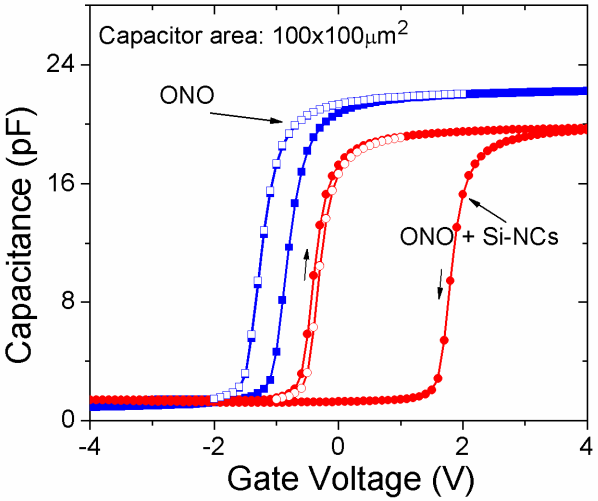

*K. Guarini et al., IEDM 2003, IBM*
*S.K.Banerjee team, IEEE EDL 28,793 (2007)*

- Structure & thickness variation of nanometer thick layers of different materials used to realize the blocking and injection layers

# ULE-IBS NPs in High-*k* Dielectrics

- Si-NPs embedded in 6nm Si3N4



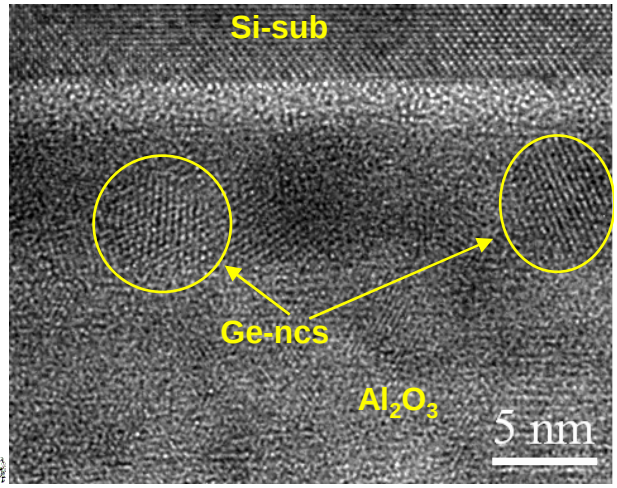



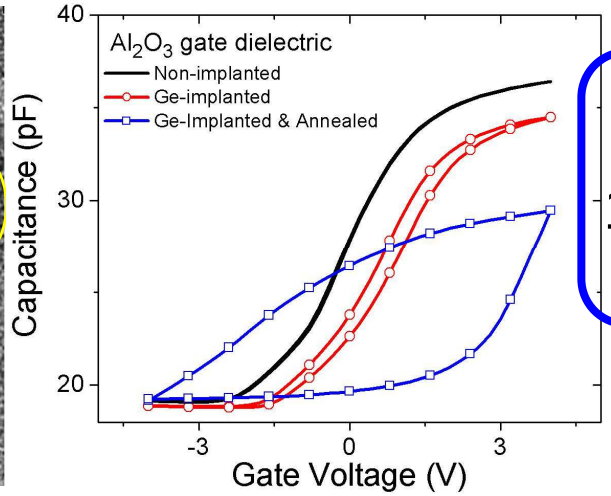

**MONOS NVM cells**

1KeV, $1.5\times10^{16}Si^{+}cm^{-2}$, 950°C 30min $N_2$

*V.Ioannou et al, Nanotechnology 18, 215204 (2007)*

- Ge-NPs embedded in 7nm ALD Al2O3



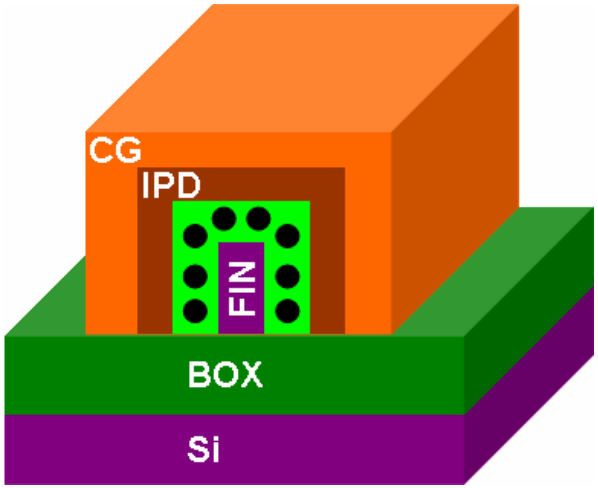

**NP-NVM cells**

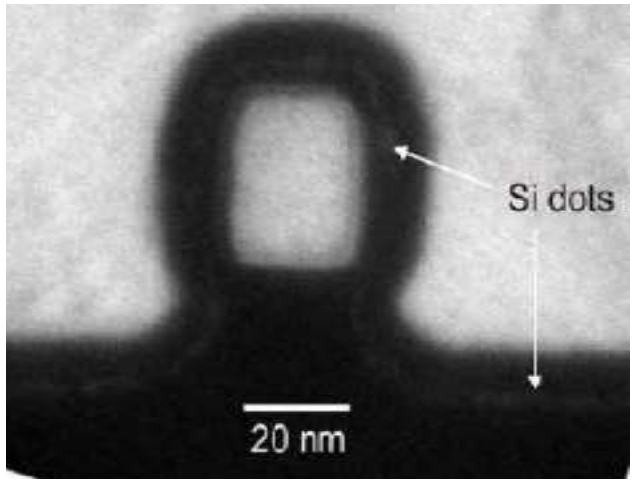
1KeV, $0.5\times10^{16}Si^{+}cm^{-2}$ 800°C 20min $N_2$

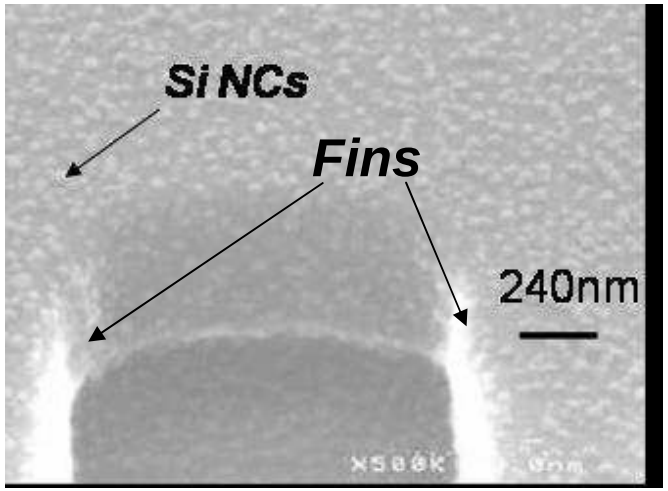
*P.Dimitrakis et al., to be published*

# Emerging cell architectures

➢Trigate FinFET FLASH memory cells



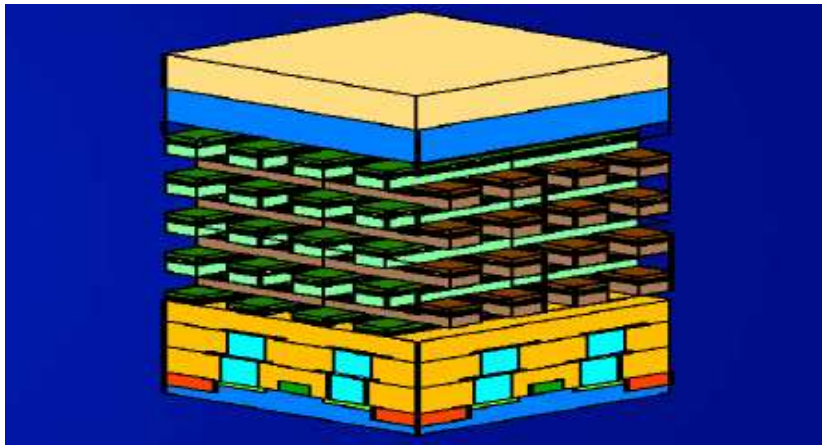




*S.Lombardo et al, IEDM 2007*

➢Cross-point 3D architectures

Effective cell area: $mF^2/N$
$mF^2$: cell area
N: number of layers



# Bibliography

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