Nanoparticle Memories: CMOS, Organic and Hybrid approaches

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IMEL/NCSR "Demokritos"

"Winter School on Nanoelectronic and Nanophotonics"

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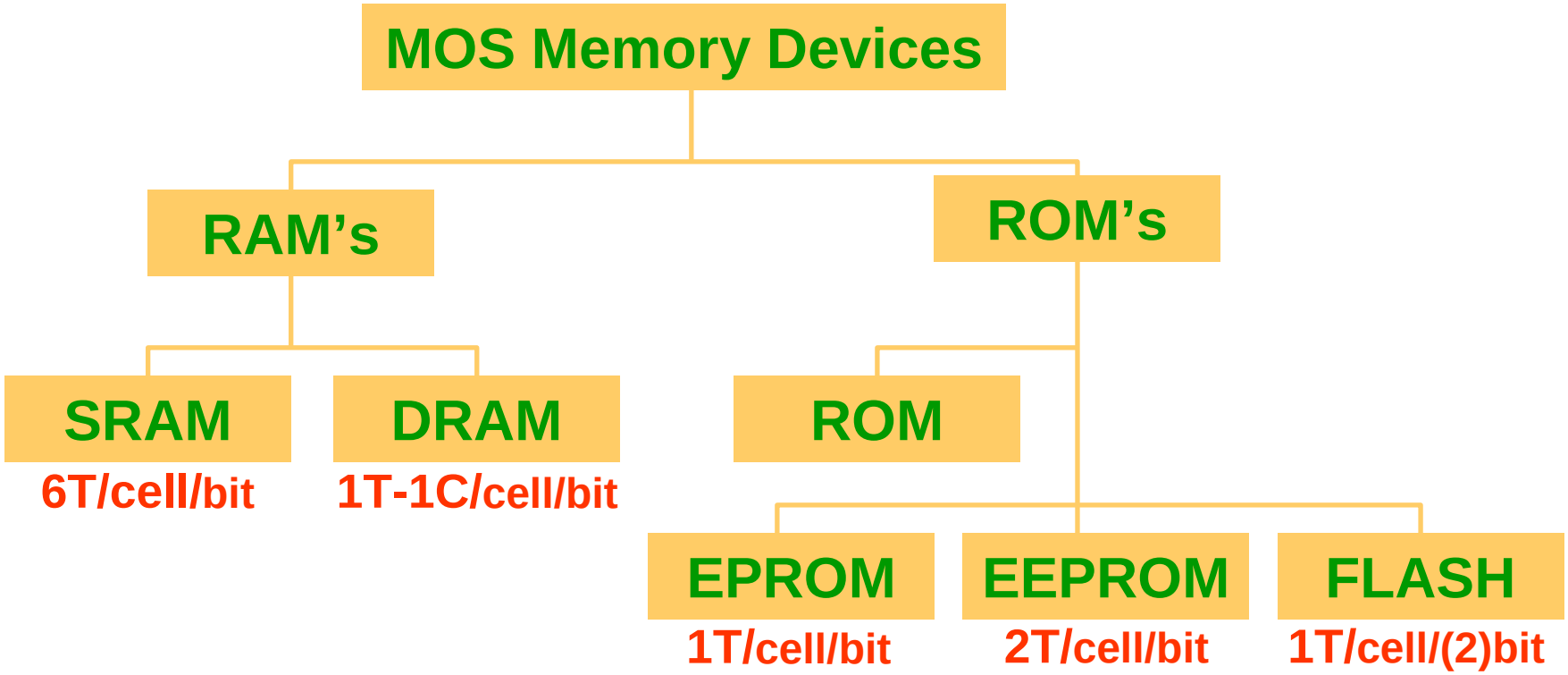
Outline

- 11:50 – 12:40 (1st Hour)
  - Introduction to Metal-Oxide-Semiconductor (MOS) devices
  - Introduction to Memory Technology (Flash NAND & NOR)
  - Flash scaling issues
  - Emerging memory devices (CMOS & CMOS)

- 14:00 – 15:50 (2nd Hour)
  - NP-NVM: CMOS Approach

- 16:00 – 16:50 (3rd Hour)
  - NP-NVM: Organic approach
  - NP-NVM: Hybrid approach

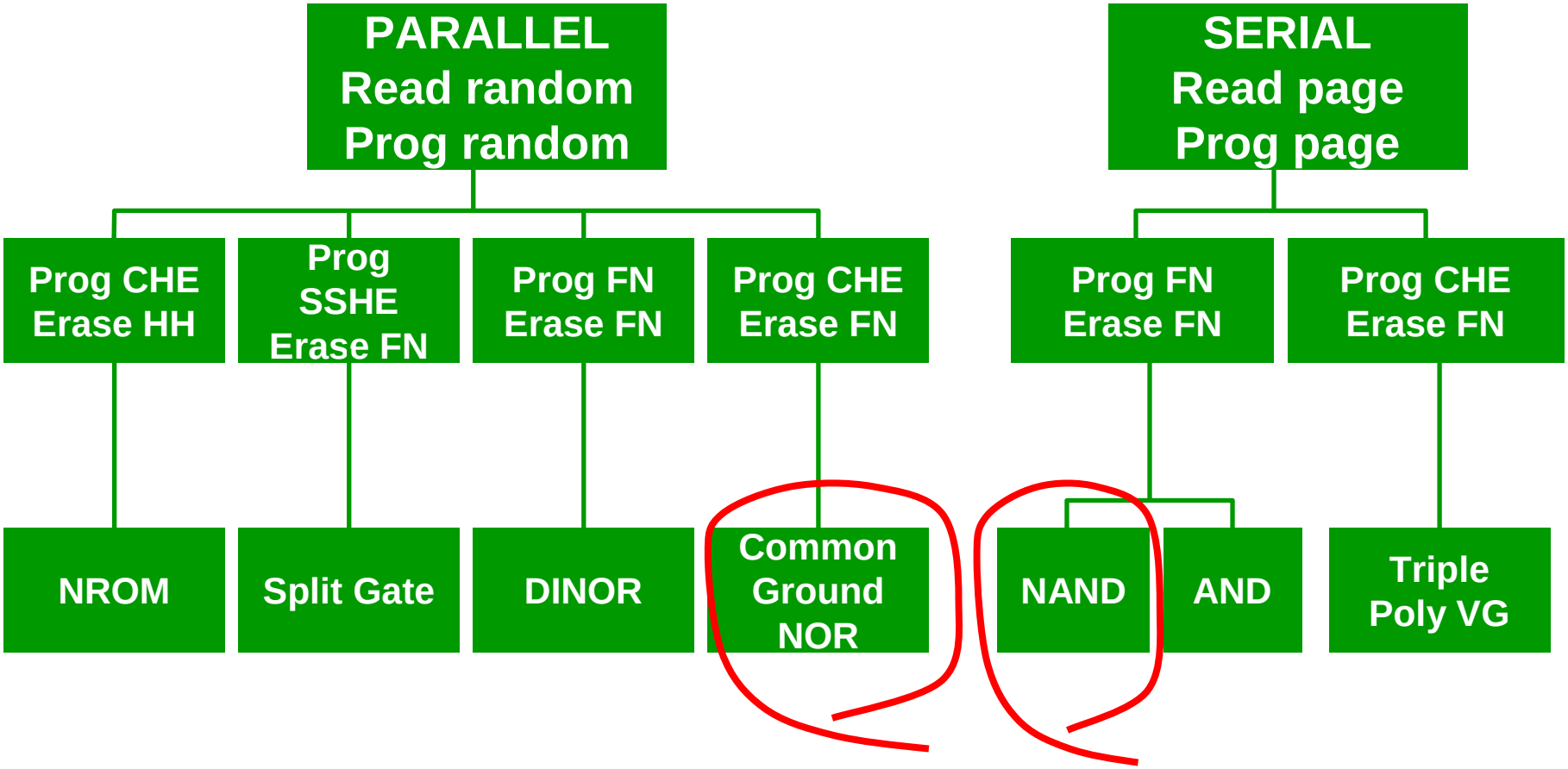
MOS Memory taxonomy



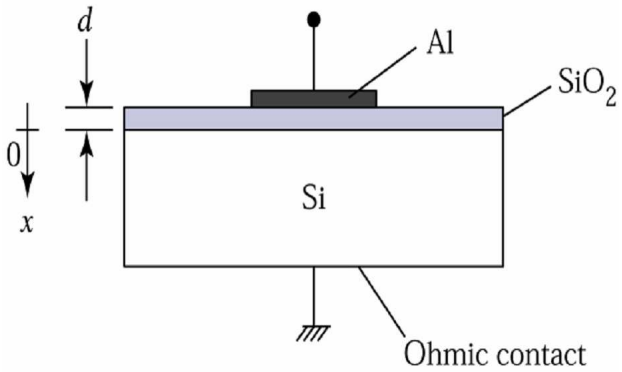
VOLATILE
Power-off: contents lost

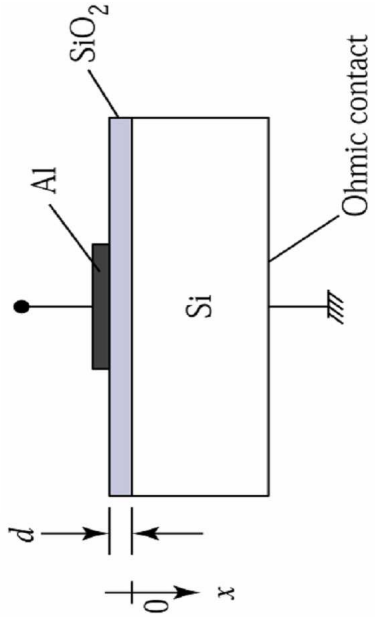
NON-VOLATILE
Power-off: contents kept

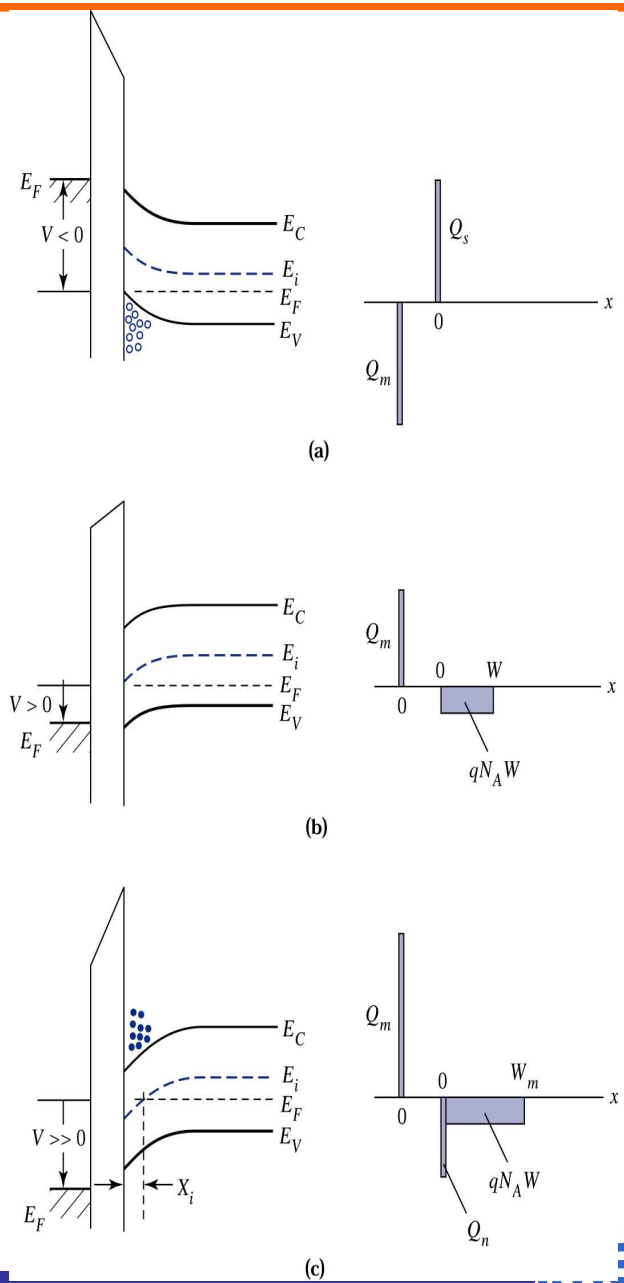
Flash Memory Architectures

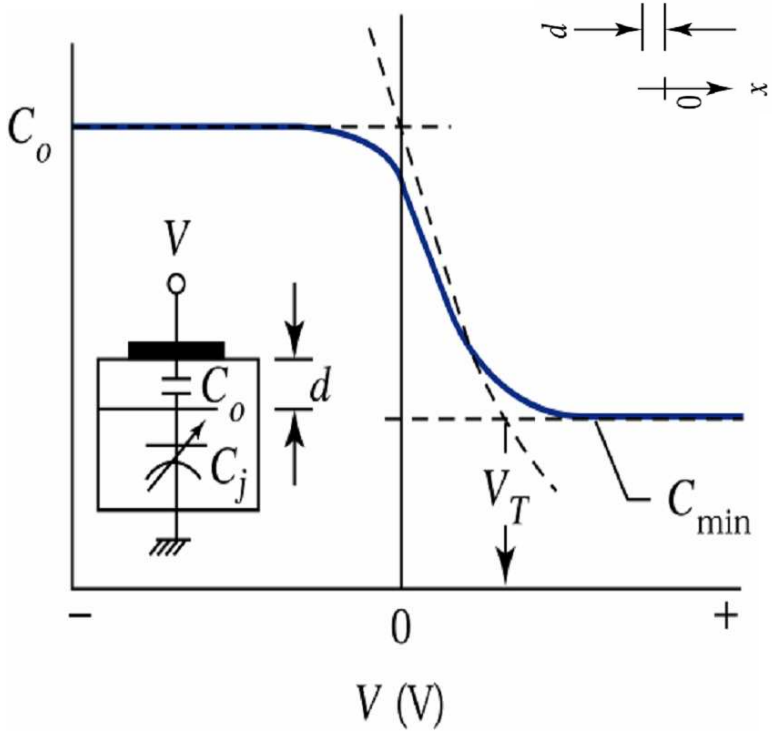


The MOS Capacitor (MOSC)

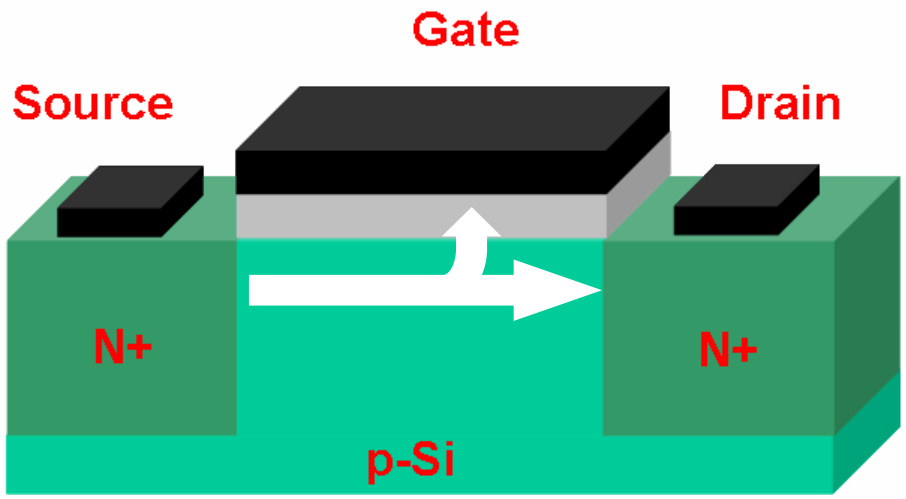




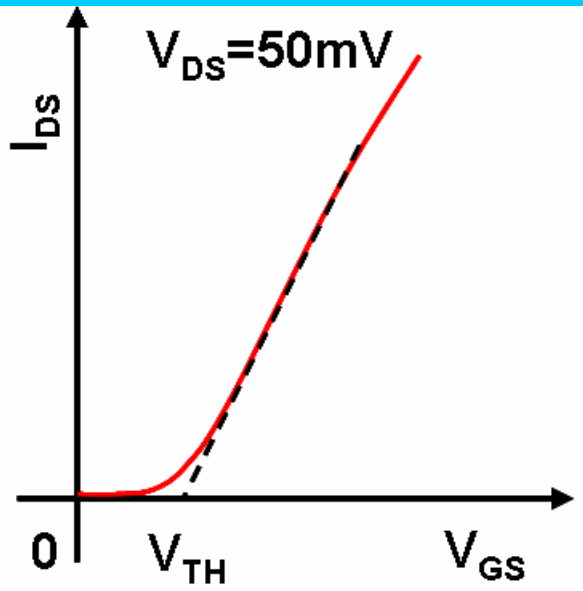




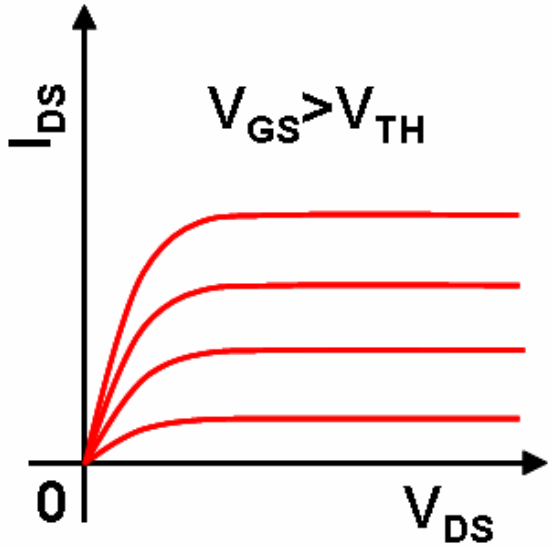
Metal-Oxide-Field-Effect-Transistor (MOSFET)



Transfer characteristic

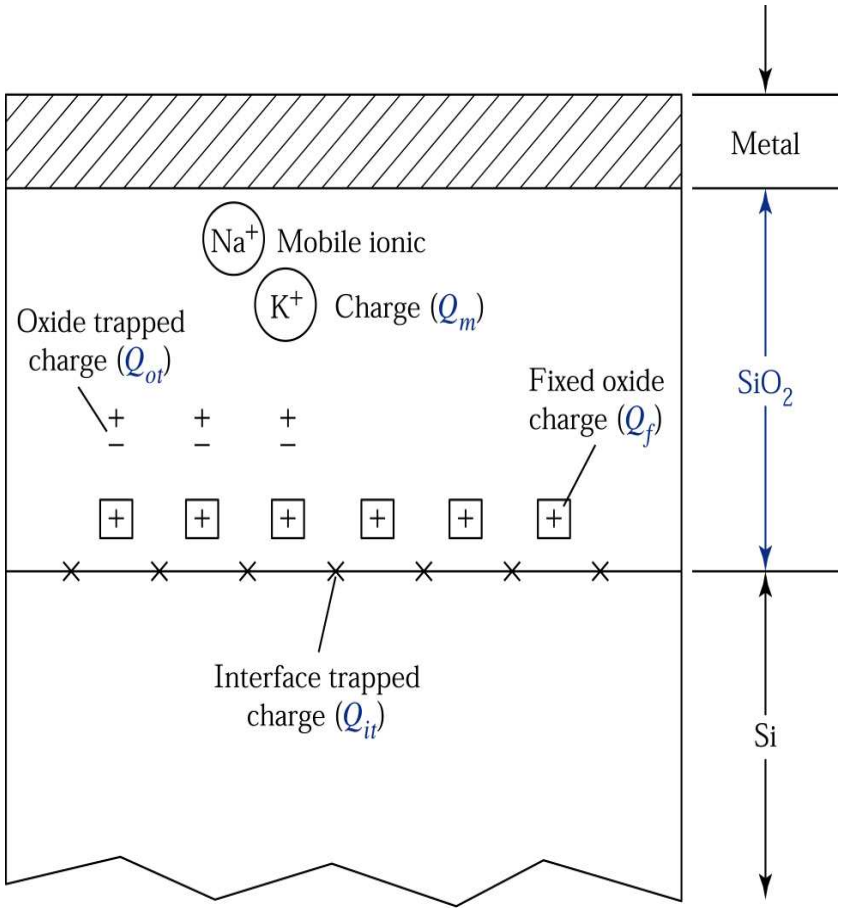


Output characteristics



Charge storage and the Floating Gate concept

- The presence of charges inside the gate dielectric modifies the surface potential at the Si/Gate dielectric interface



- The flat-band voltage or the threshold voltage of a MOSC or a MOSFET respectively are shifted towards higher or lower values depending on the polarity of the charges, i.e. electron or holes respectively

$$V_{FB} = \phi_{ms} - \frac{Q_{it}}{C_{ox}} - \frac{Q_m}{C_{ox}} - \frac{Q_f}{C_{ox}} - \frac{Q_b}{C_{ox}}$$

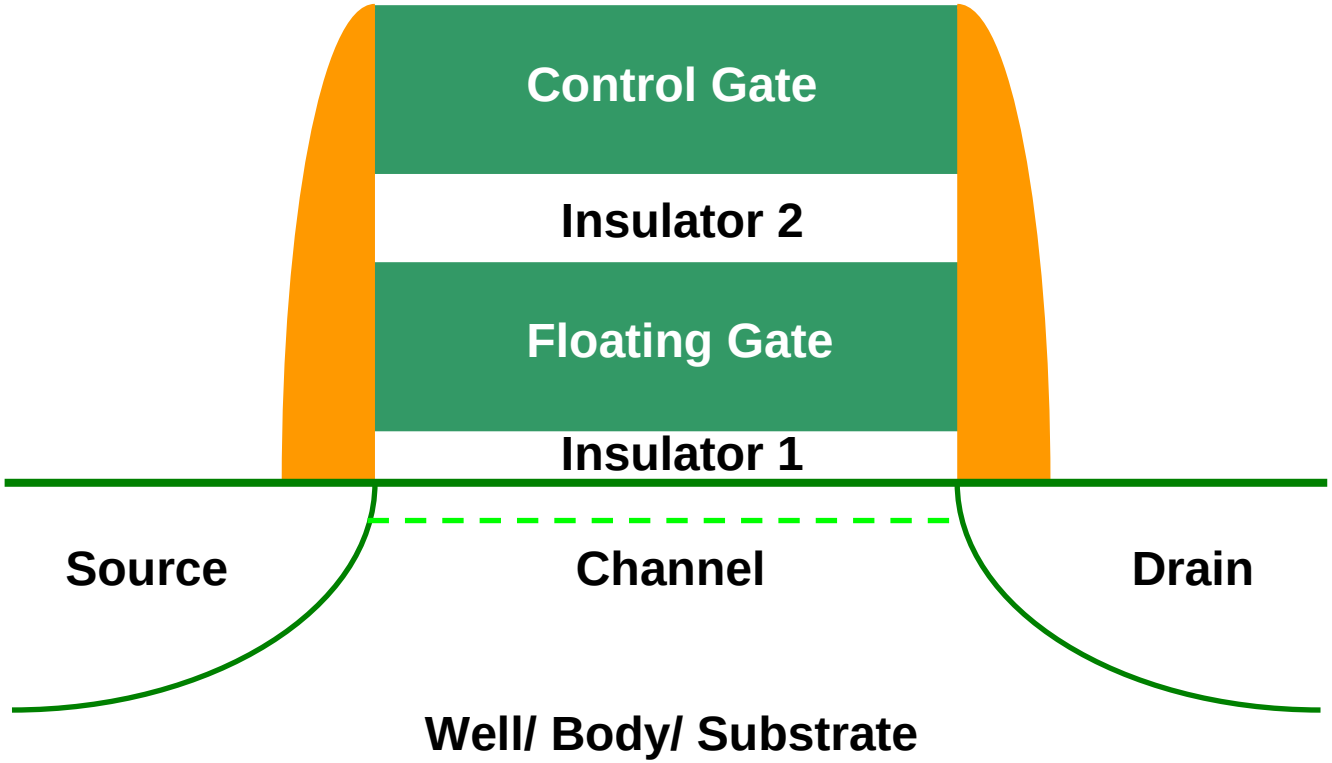
$$V_{TH} = 2\phi_F + V_{FB} \qquad \phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$Q_{XX} = \frac{1}{t_{ox}}\int_0^{t_{ox}} x\rho_{XX}(x)dx$$

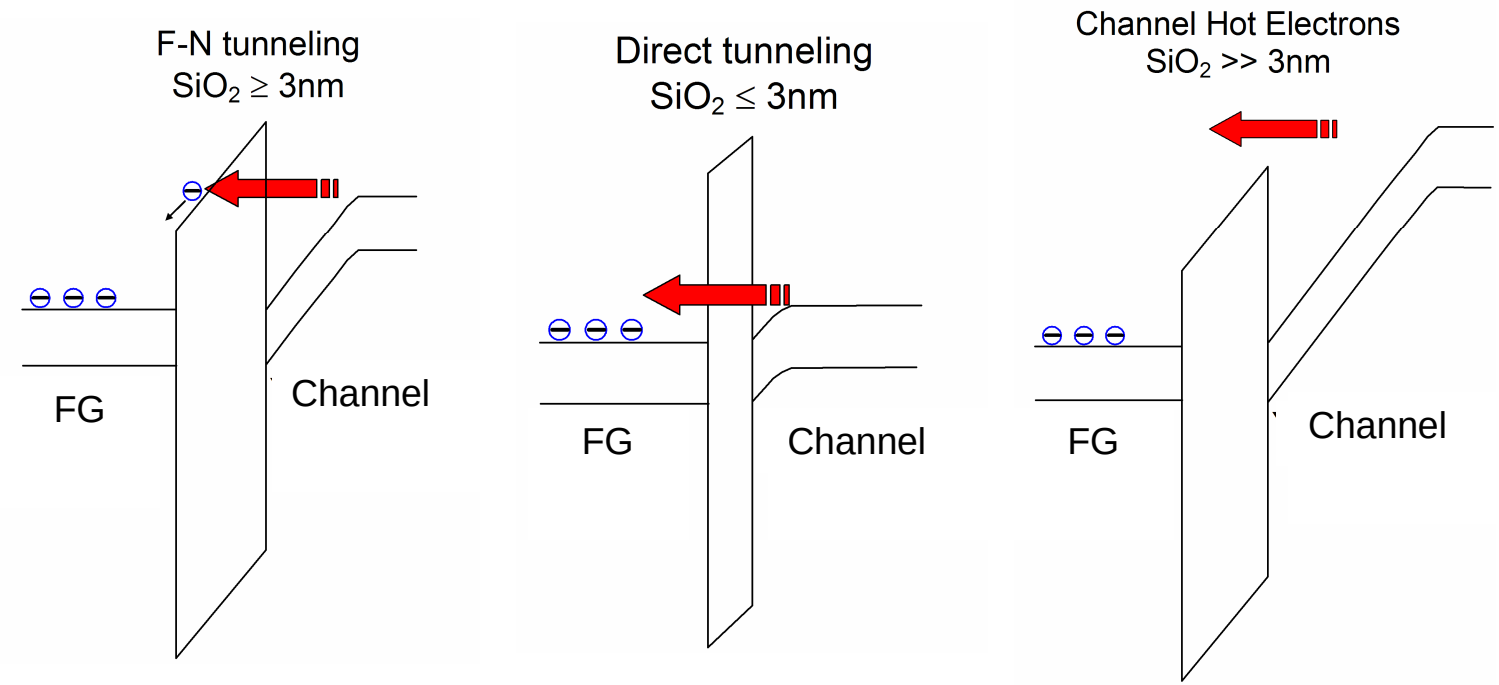
where *XX: it, m, f, b*

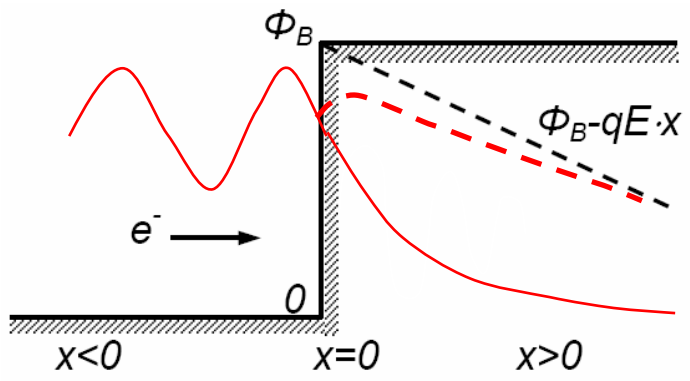
The Floating Gate MOSFET

- The first FG-MOSFET presented in 1967 by D.Kahng and S.M.Sze from Bell Labs
- The Floating gate was a highly polysilicon layer



Carrier injection mechanisms through an insulator





$$\psi(x) = \sqrt{2\kappa_0}\,\exp(-\kappa_0 \cdot x)\,,\ x \geq 0$$

$$\kappa_0 = \frac{1}{\hbar}\sqrt{2m^*(\Phi_B - q \cdot E \cdot x)}$$

Image Force Barrier lowering

$$\Delta\Phi_B = \sqrt{\frac{q^3 E}{4\pi\varepsilon_{ox}}}$$

$$U(x) = \frac{-q^2}{16\pi\varepsilon_{ox} x} - qE \cdot x$$

FN tunneling mechanism

- Tunneling through a triangular barrier $U(x)=\Phi_B - qE\cdot x$

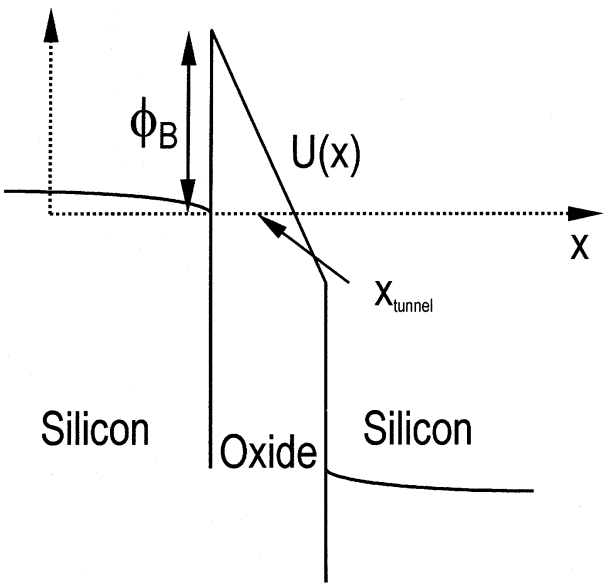
R. H. Fowler and L. Nordheim, Proc.Roy.Soc.A , 119, 173 (1928)

- For Si-SiO2 system

M. Lenzlinger and E. H. Snow, J.Appl.Phys. 40, 278 (1969)

Transmission coefficient

$$T_{tri}(E) = \exp\left[-\frac{8\pi\sqrt{2m_{ox}^*}}{3hq}\cdot\frac{(\Phi_B - E)^{3/2}}{E_{ox}}\right]$$

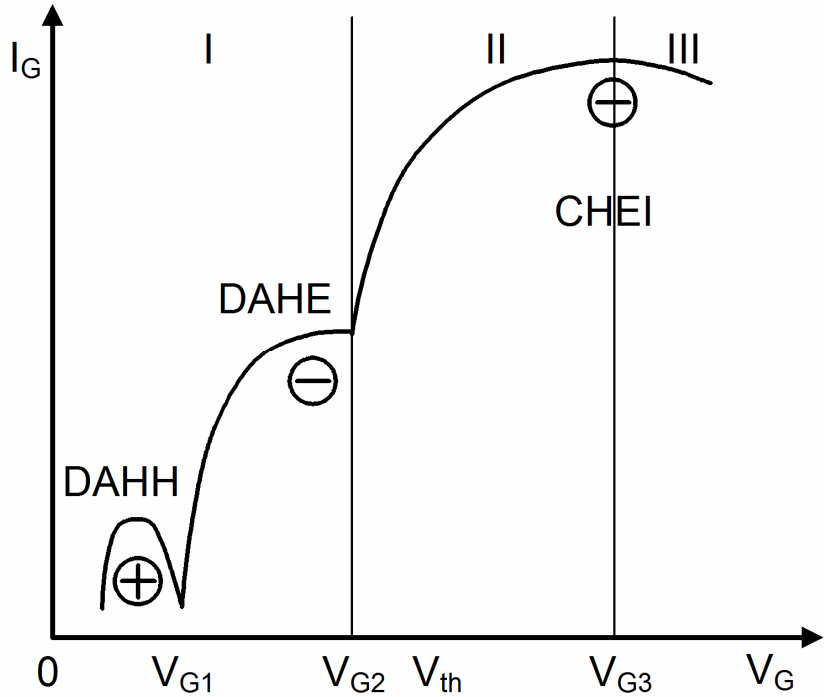


Current density

$$J_{FN} = A\cdot E_{ox}^2 \exp(-B/E_{ox})$$

$$A = 1.54\times10^{-6}\frac{(m_e/m_{ox}^*)}{\Phi_B}[\mathrm{A/V^2}] \qquad B = 6.83\times10^7\sqrt{(m_{ox}^*/m_e)\cdot\Phi_B{}^3}[\mathrm{V/cm}]$$

Hot-carrier Injection



Ch.51, *CRC VLSI Handbook*, 2000

$$I_G = \int_o^L I_D \frac{P1 \cdot P2 \cdot P3}{\lambda_r} dx$$

The Lucky electron model

C. Hu, *IEDM Tech. Dig.*, p. 22, 1979

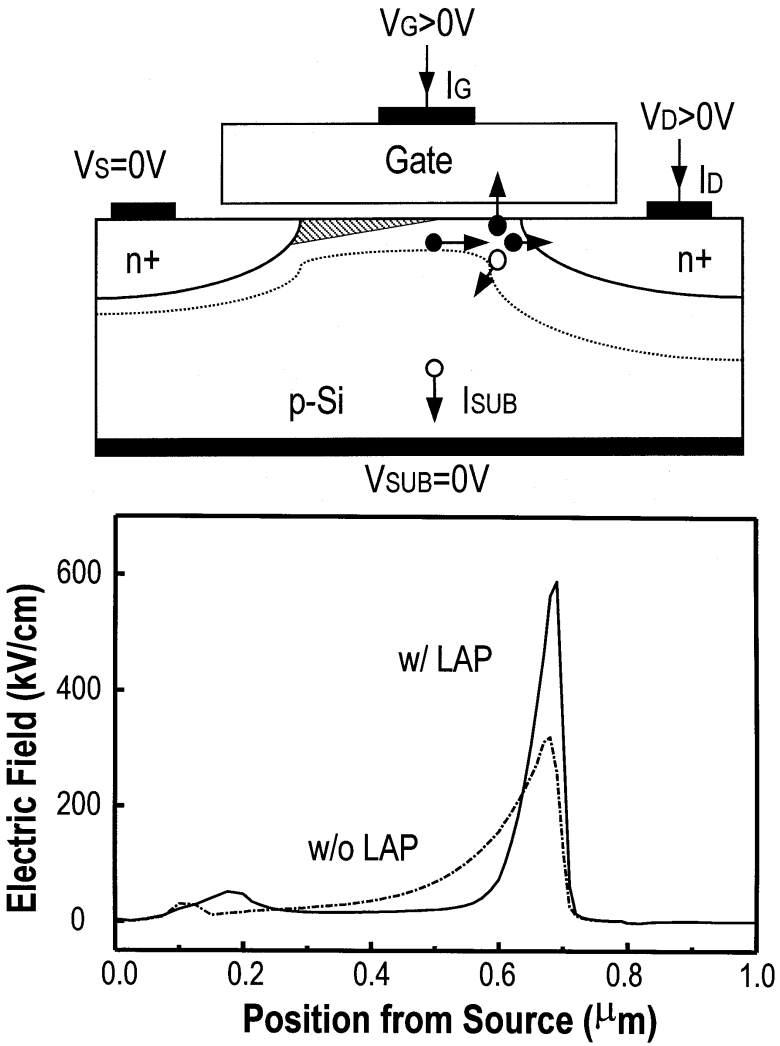
- the probability of a hot electron to gain enough kinetic energy and normal momentum
- the probability of not suffering any inelastic collision during transport to the Si–SiO2 interface, and
- the probability of not suffering collision in oxide image potential well

$$P1 = \exp\left(-\frac{\Phi_B}{E \cdot \lambda}\right) \qquad P3 = \exp\left(-\frac{y_0}{\lambda_{ox}}\right)$$

$$P2 = \frac{\int_0^\infty n(y) \exp\left(-\frac{y}{\lambda}\right) dy}{\int_0^\infty n(y) dy}$$

Channel Hot-Electron Injection

Mechanism description



Topics

- Special technology process for Source/Drain fabrication in order to
  - enhance the injection efficiency, i.e. low angle p-pocket
  - enhance the device integrity
- The shrinkage of the gate length increases the lateral electric field ⇒ CHEI enhancement

FN or CHEI?

Comparison of FN and CHEI as programming scheme for stacked-gate devices

FN Tunneling Injection Scheme

- Low power consumption
  - Single external power supply
- High oxide field
  - Thinner oxide thickness
  - Higher trap generation rate
  - More severe READ disturbance
- Slower programming speed

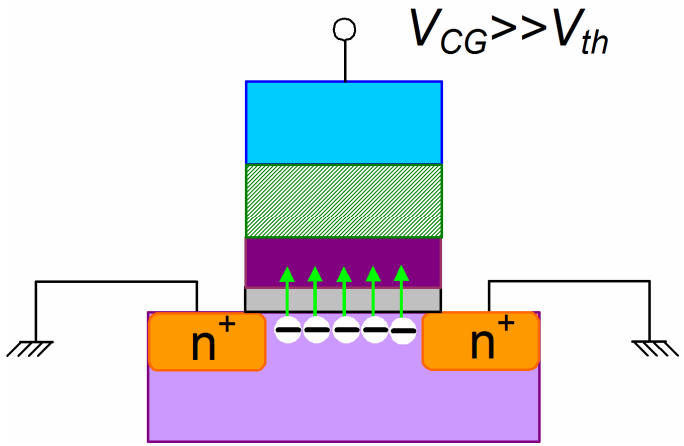
CHEI Scheme

- High power consumption
  - Complicated circuitry
- Lower oxide field
  - Oxide can be thicker
  - Higher oxide integrity
  - Low READ disturbance
- Faster programming speed

Current FG-NVM cell – Principle of Operation

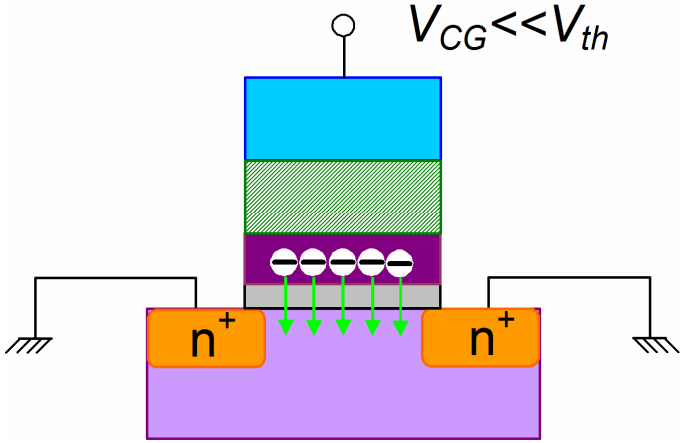
"WRITE" Operation

Bit "1"

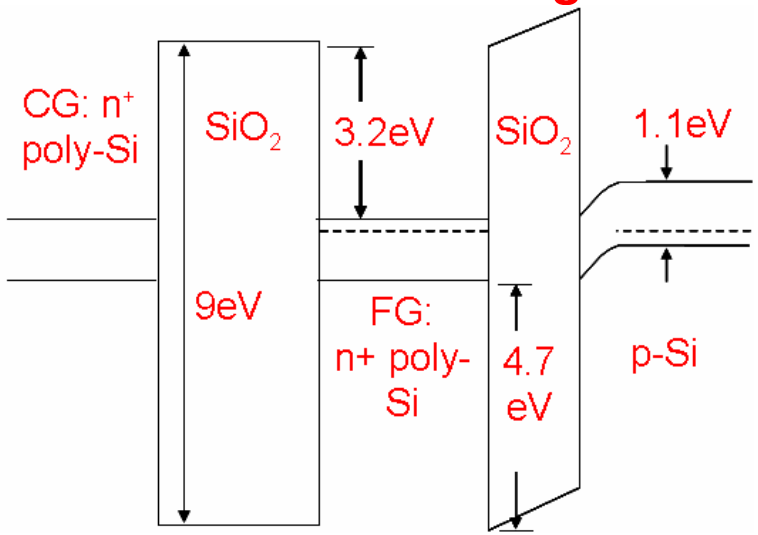


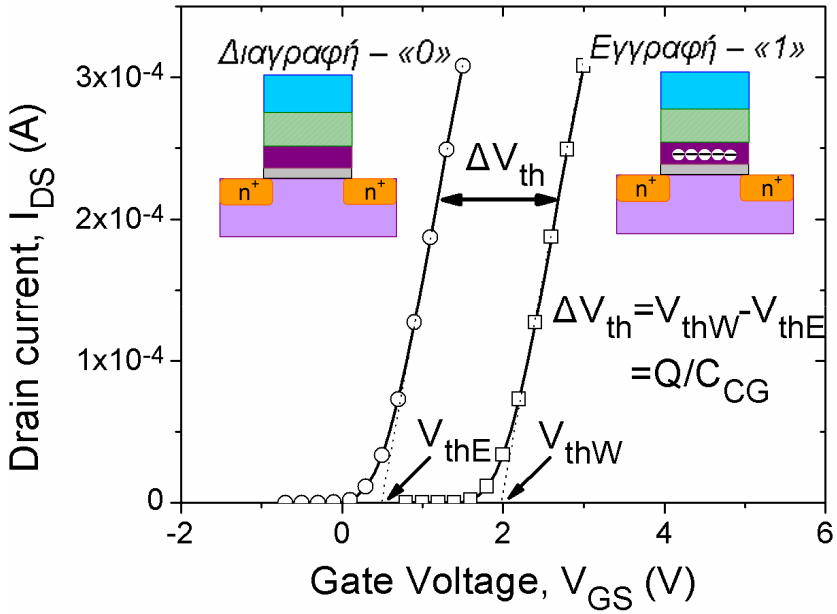
"ERASE" Operation

Bit "0"



FG structure: Band Diagram

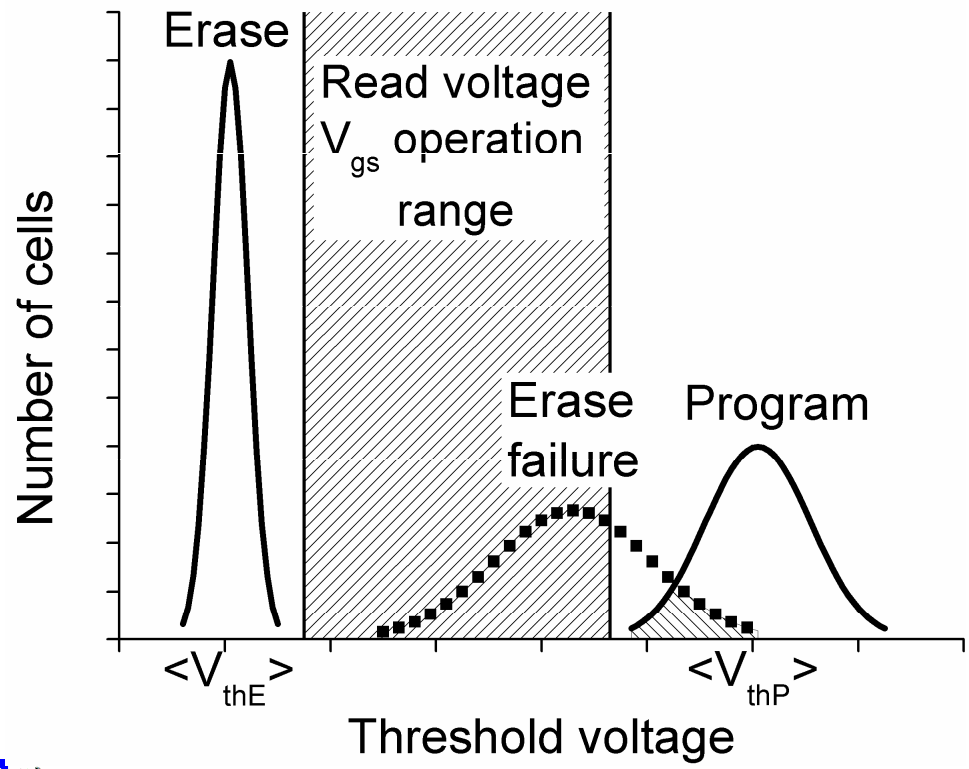


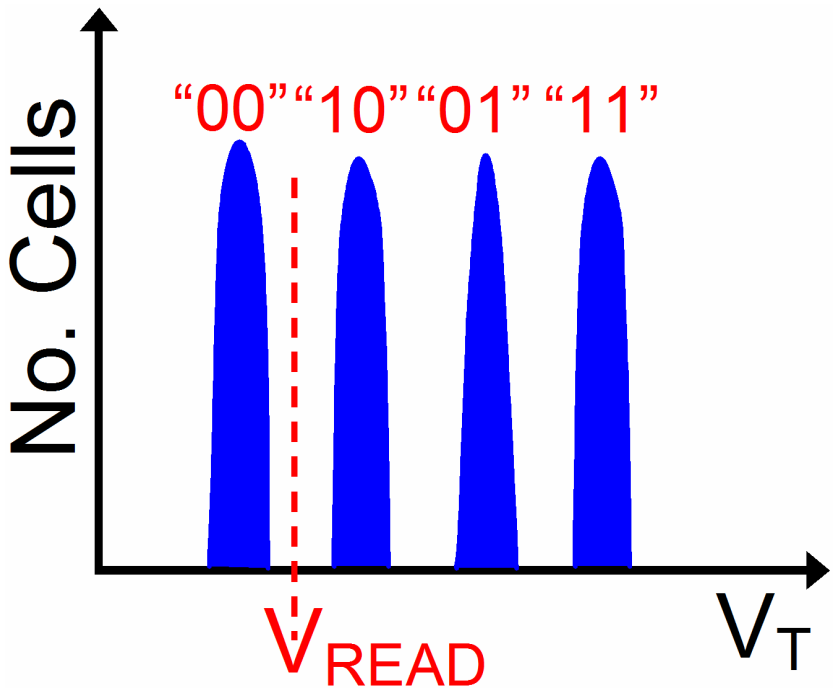


Memory Array – Multi-level Cell (MLC)

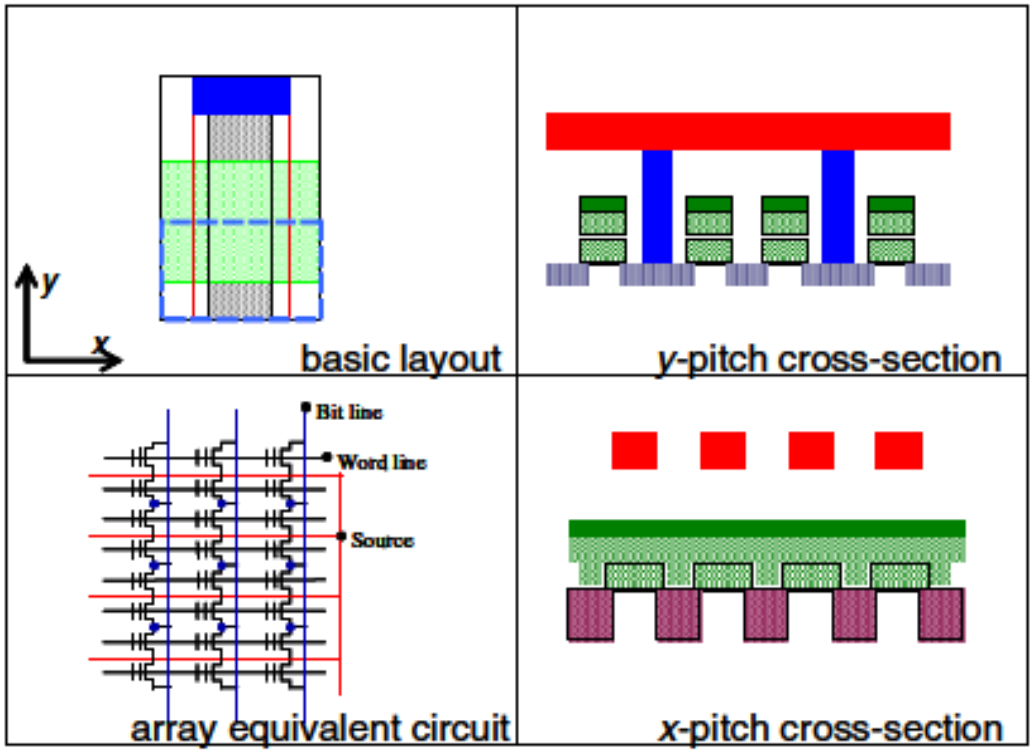
- V_{th} at ERS or PGM states is distributed around a mean value
- Cells' failure cause decrease the READ voltage region
- READing wrong information

- More than 1bit/cells
- $M=2^N$ M: memory levels (states), N: number of bits/cell
- N=2,3 in market
- N=4 soon





NOR Flash

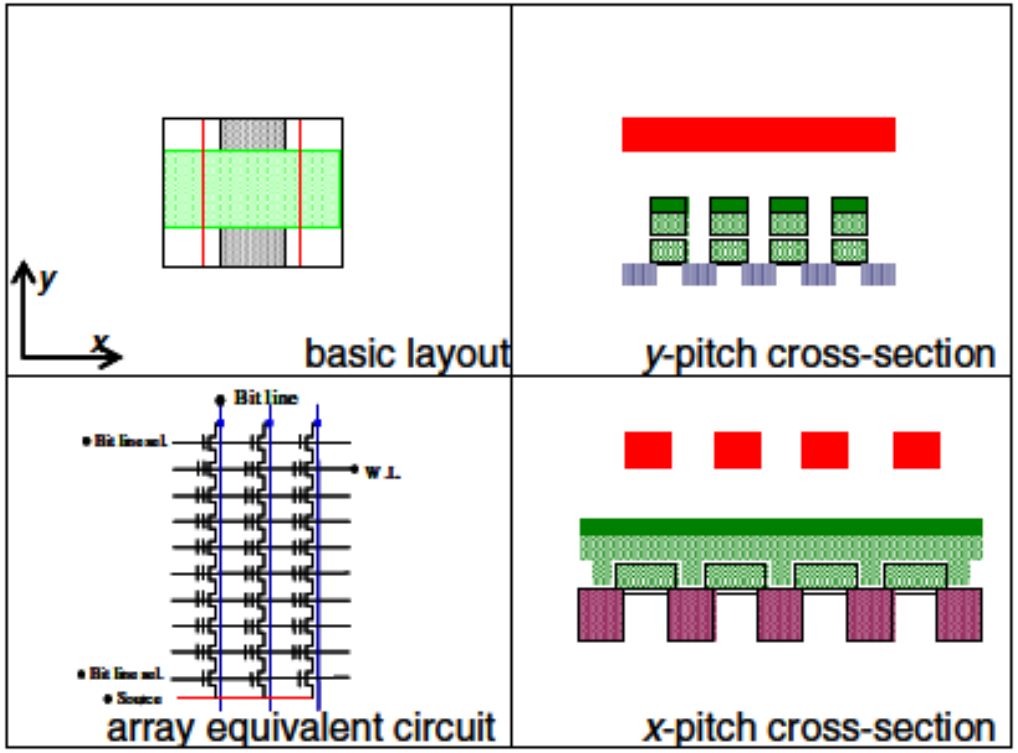


NOR	PGM	ERS
Mechanism	CHE	FN
V wl (V)	8 – 10	-8
V bl or body (V)	4 – 5 (bit line)	6 – 8 (body)
Pulse (μs)	1	10^5
I read (μA)	20-40	20-40
Throughput	0.5MB/s	

<u>130nm Technology Node</u>

✓Tunnel oxide: 9-10nm
✓ ONO EOT: 15nm
✓ Cell gate length: 200nm

NAND Flash



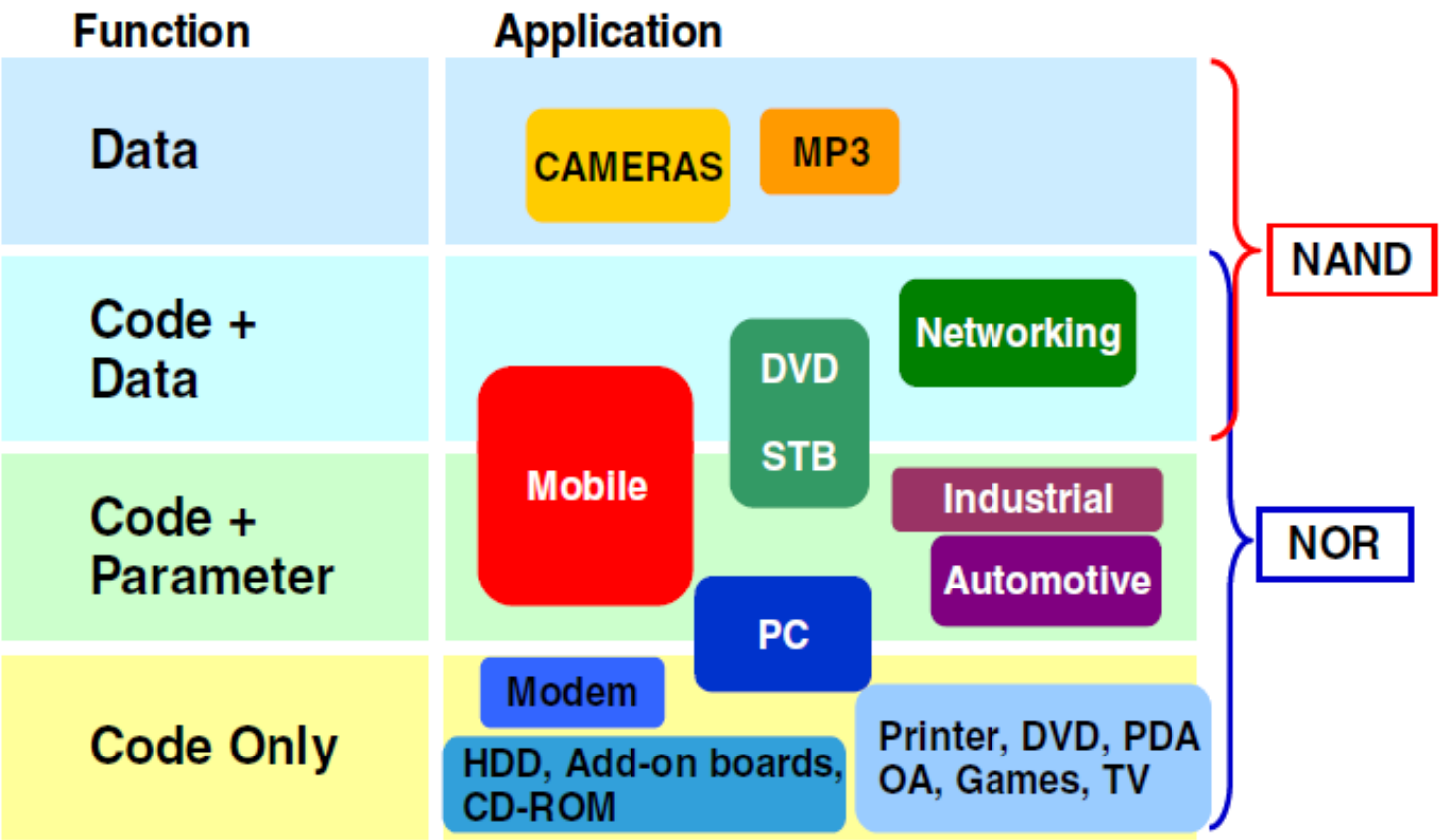
NAND	PGM	ERS
Mechanism	FN	FN
V wl (V)	18 – 20	0
V bl or body (V)	0 (body)	18-20 (body)
Pulse (μs)	300	$2x10^3$
I read (μA)	0.3-0.5	20-40
Throughput	10MB/s	

130nm Technology Node

✓Tunnel oxide: 7-8nm
✓ ONO EOT: 15nm
✓ Cell gate length: 130nm

Memory Type	Main characteristics	Suitability	Applications
DRAM	➢Volatile ➢Small cell/die size ➢Slower than fast SRAM	Systems with a relatively large amount of memory, where memory cost is critical	Main memory in PC, workstation and file server applications; networking and communications systems; graphics and peripheral sub-systems
SRAM	➢Volatile ➢Large cell/die size ➢Fast or low power	Systems with a relatively small amount of memory, where memory performance or low power are critical.	Cache memory in PC and workstations applications (fast SRAM); high-speed networking systems (fast SRAM); hand-held devices (low-power SRAM)
Flash (code-storage type, NOR)	➢Non-volatile ➢Large cell/die size ➢Fast random access ➢Slow block read/write access*	Data that must be retained when power is turned off and is necessary for MCU/MPU function and operating system storage.	Code storage for PC BIOS, cellular phones and networking equipment
Flash (data-storage type, NAND)	➢Non-volatile ➢Small cell/die size ➢Slow random access ➢Fast block read/write access*	Data which must be retained when power is turned off and is necessary for application software and user data	Data storage in digital cameras (digital film) and audio/voice recorders (tape replacement); hard/floppy disk drive replacement in portable applications

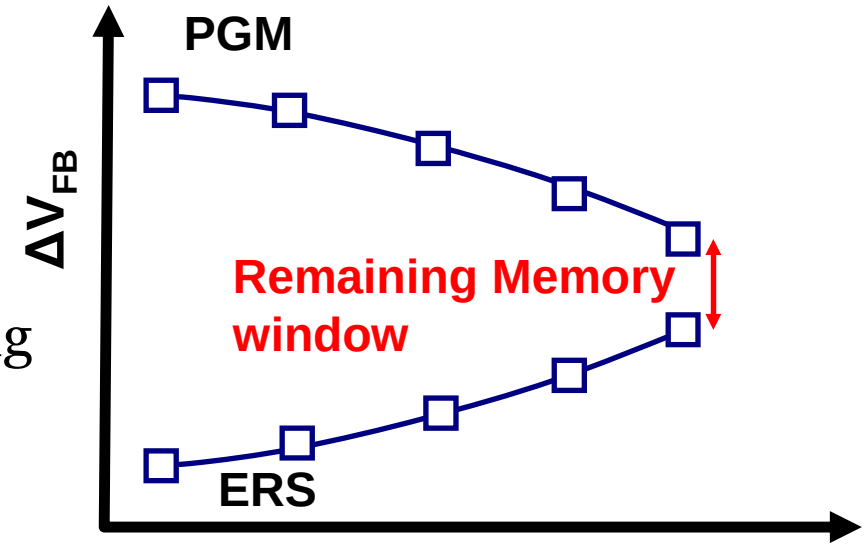
Memory Applications Trends

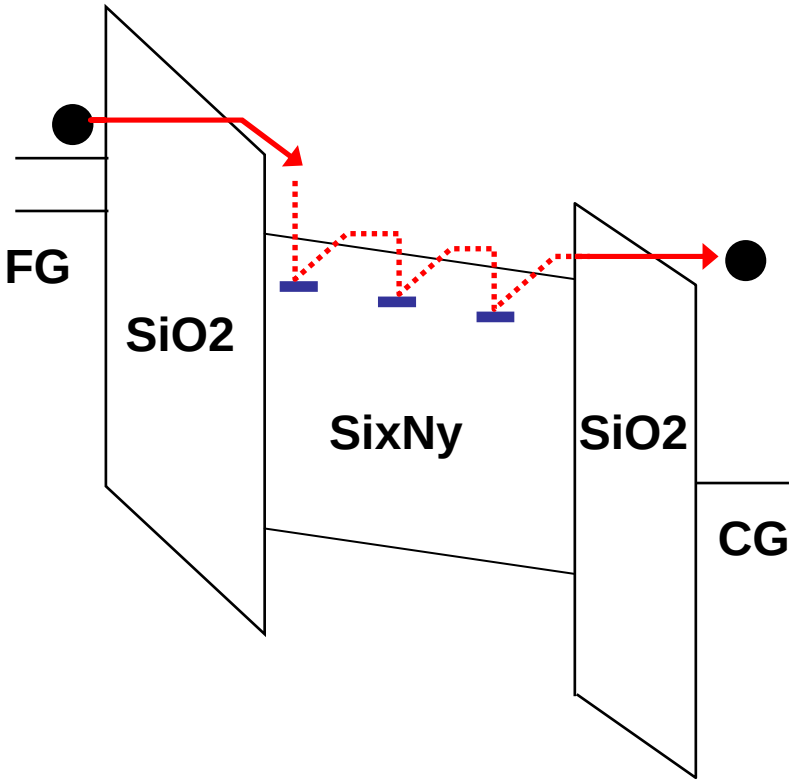


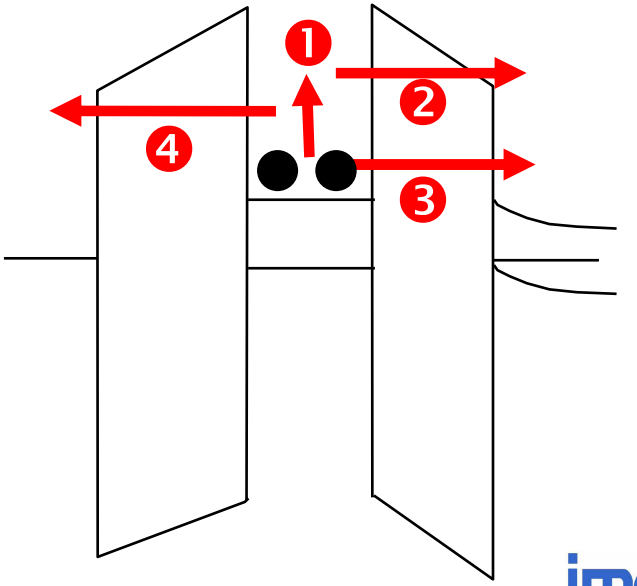
Data Retention

Possible causes of charge loss are:

- ❑ defects in the tunnel oxide ❶❷❸
- ❑ defects in the interpoly dielectric ❹
- ❑ mobile ion contamination
- ❑ detrapping of charge from insulating layers surrounding the FG

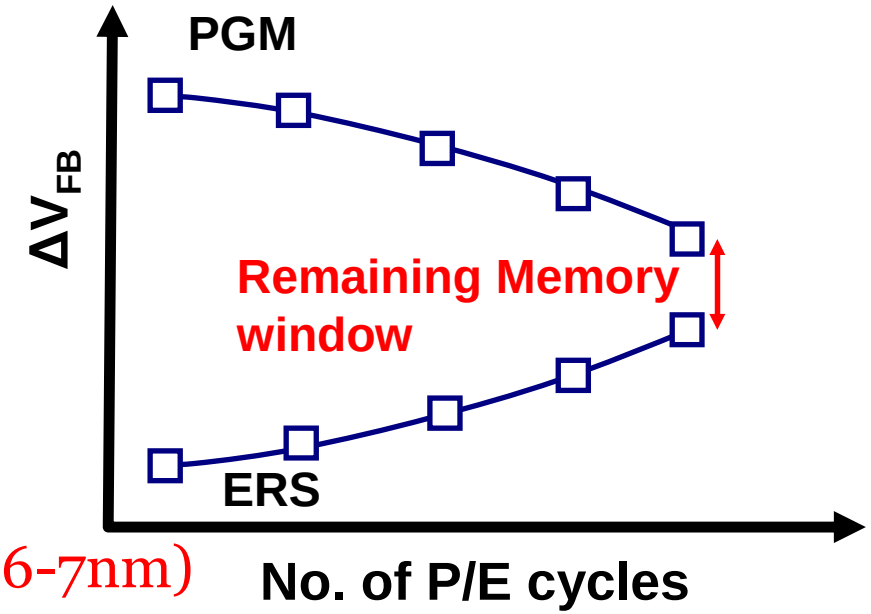






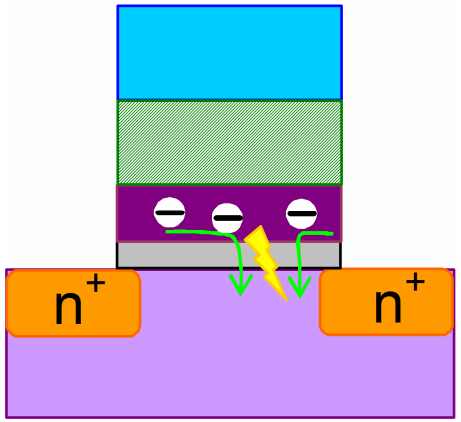
Cycling Endurance and Data Retention

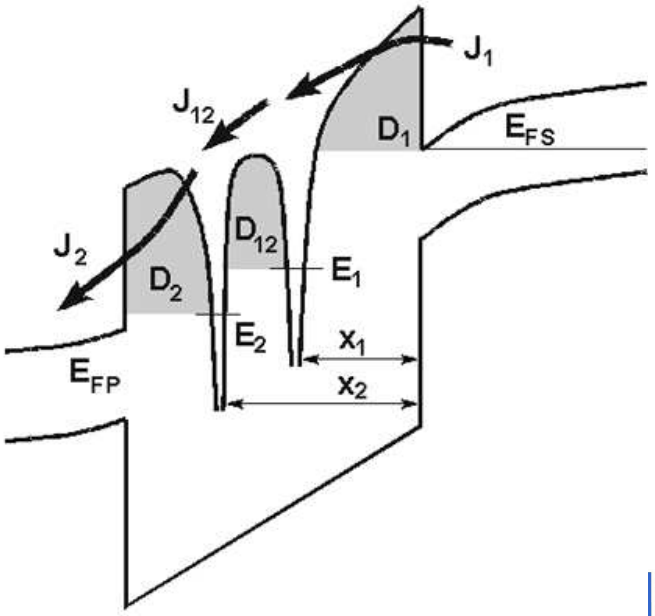
- Data loss due to SILC (≤8-9nm)
  - Creation of defects due to cycling (10^5P/E, high voltage operation)
  - SILC is due Trap Assisted Tunnelling



- Data loss due to Direct Tunneling (≤6-7nm)
  - Direct tunnel time (20% data loss)

4nm → 4.4min, 5nm → 1day, 6nm → 7mons - 6yrs

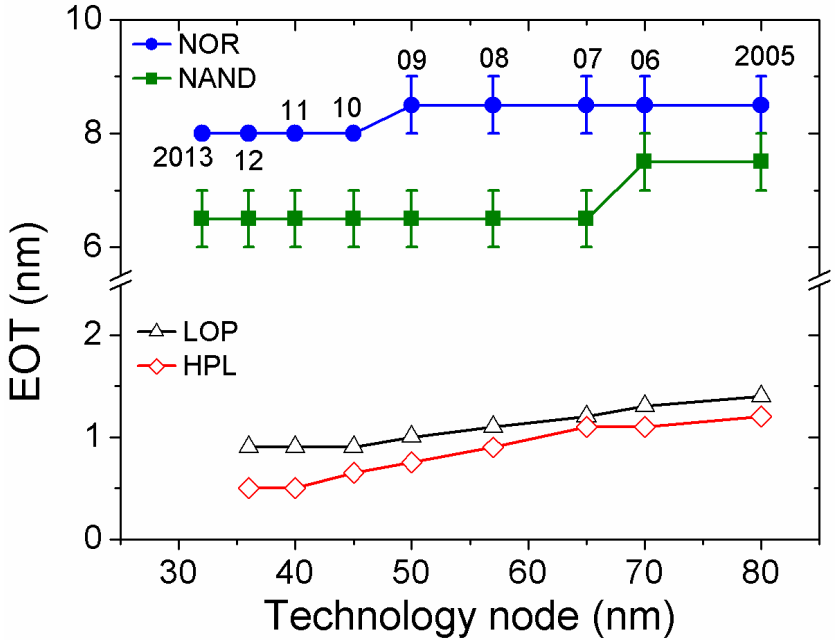


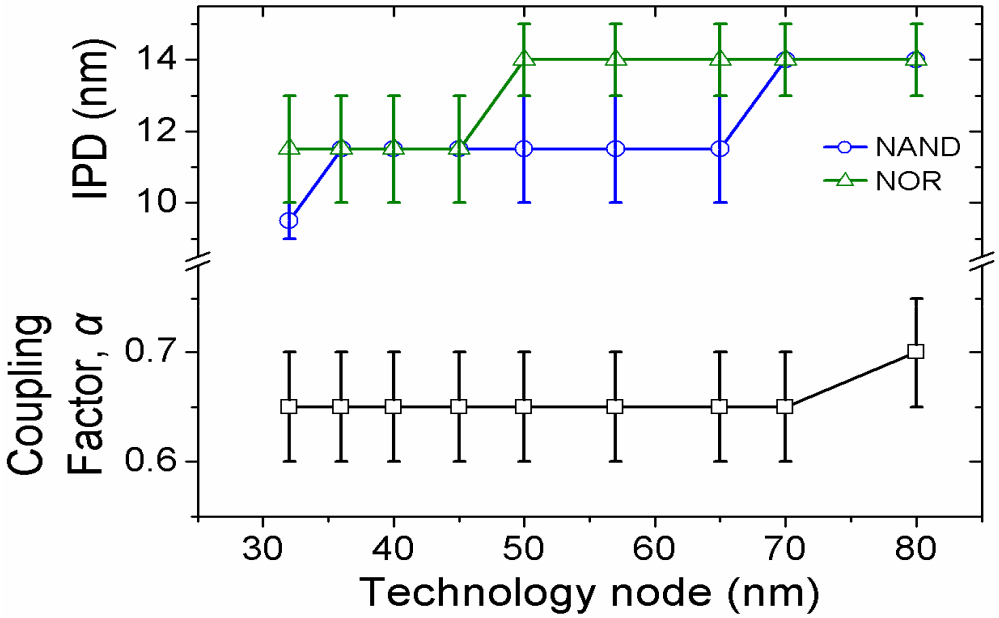


Scalling Issues

Logic-Memory: Technology Convergence is necessary

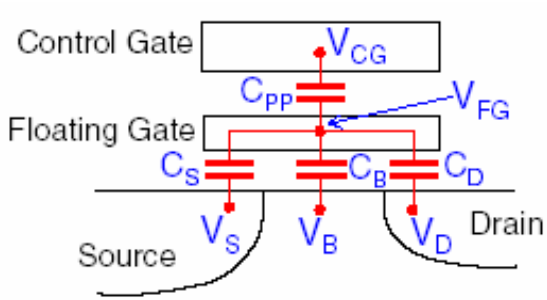
- TO thickness reduction
- Higher coupling factor a is necessary

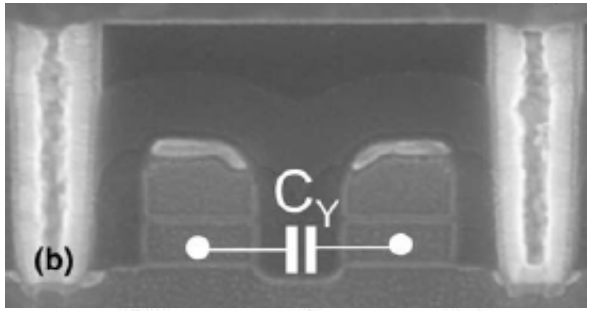


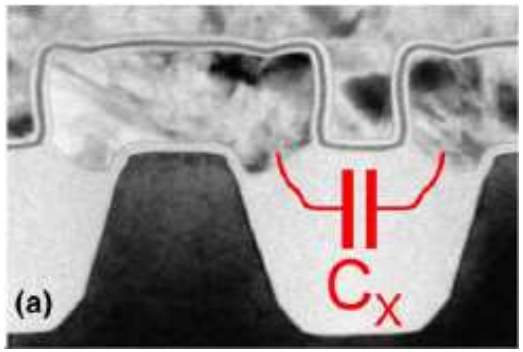


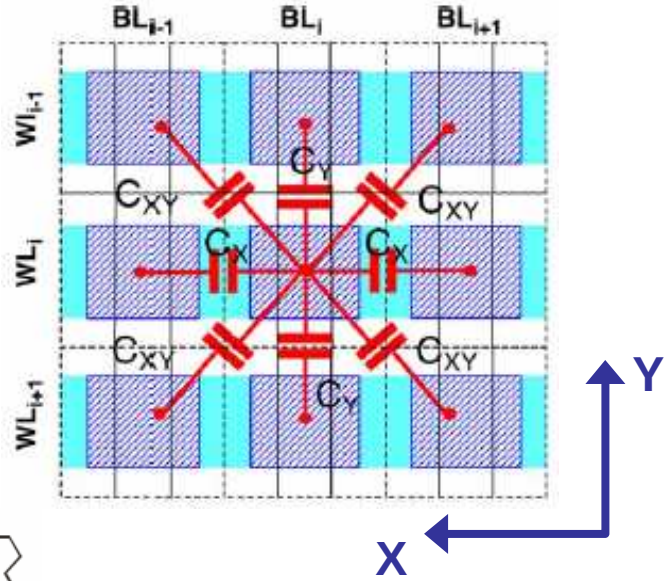
ITRS 2005

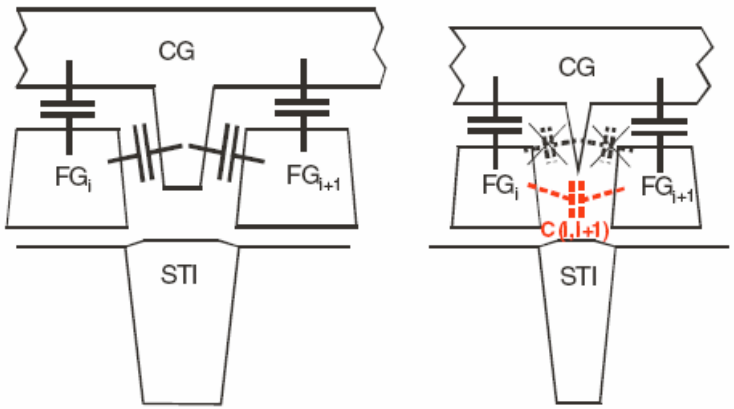
FG-cell Interference – Crosstalk









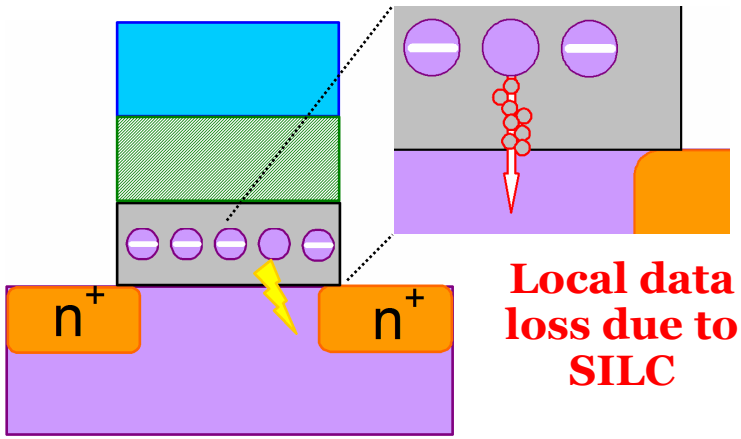


Govoreanu et al., SSE 49 (2005) 1841

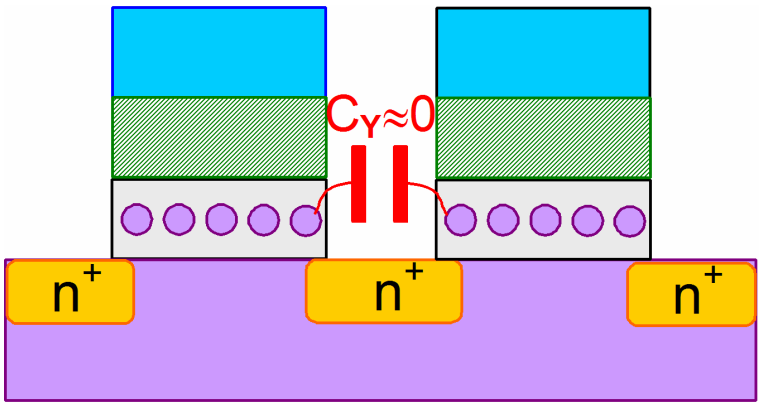
...and the answer is

Discrete Charge Storage

Loss nearby the storage node

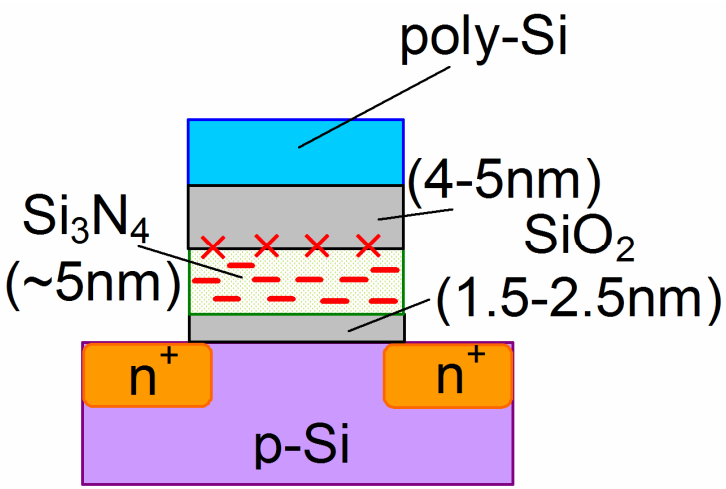


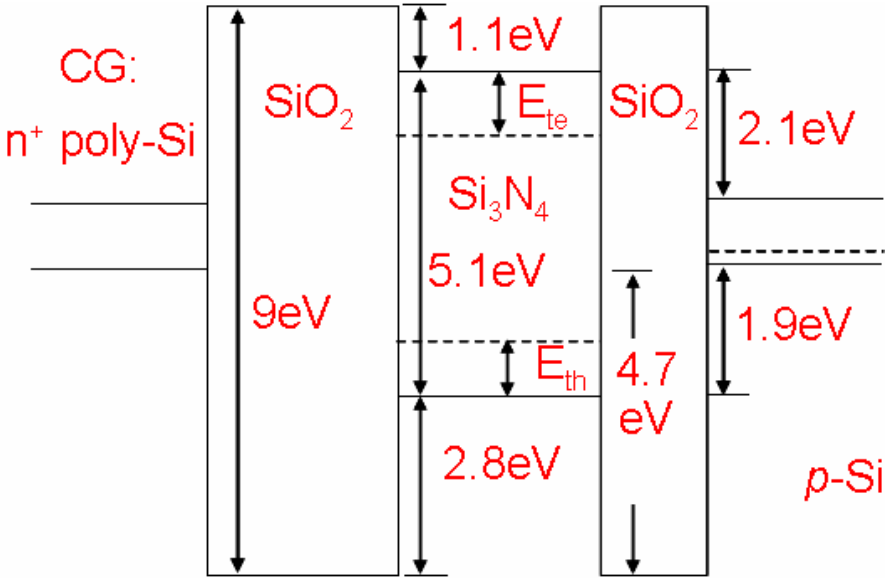
Minimization of crosstalk



Emerging "FG-Memory" Devices

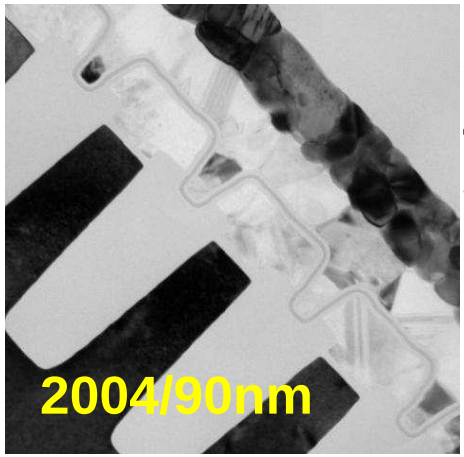
- Barrier Engineering FG-NVM
  - VARIOT
  - Crested barrier
- Charge-trapping memories
  - SONOS
  - BE-SONOS
  - TANOS
  - MAHOS
- Nanoparticle memories
  - Semiconductor
  - Metallic
  - Crystalline or amorphous





...but conventional Flash is still alive!

- Intel & Micron joint venture IM Flash Technologies announced mass production of 34nm Flash, 32Gbits NAND
- Approximately 1.6 terabytes of NAND per wafer!



56nm	3-bit/cell	4181nm^2/bit
43nm	2-bits/cell	3698nm^2/bit
34nm	2-bit/cell	2312nm^2/bit

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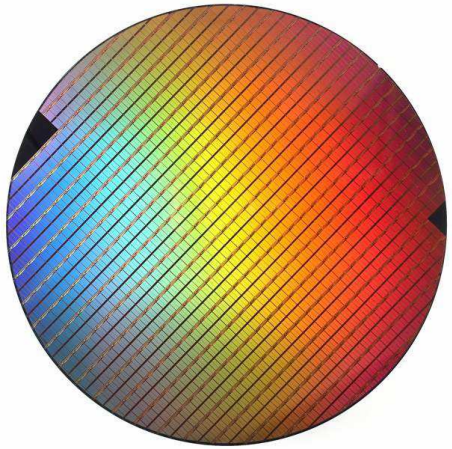

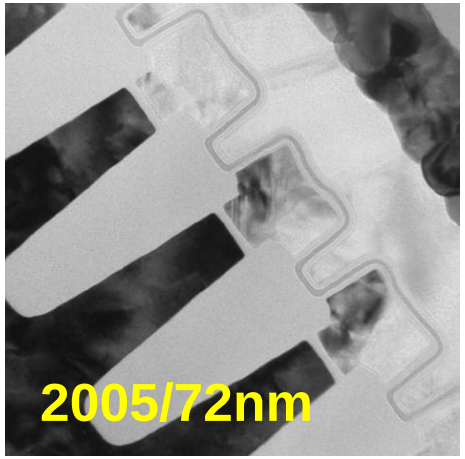

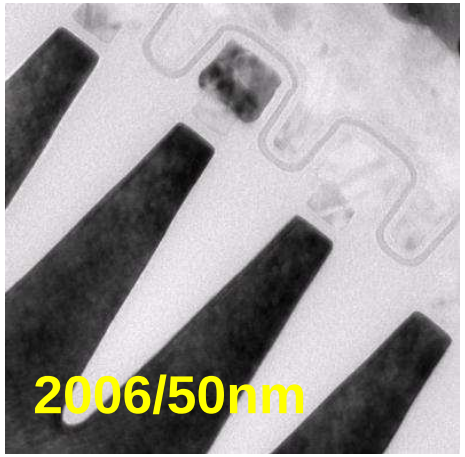

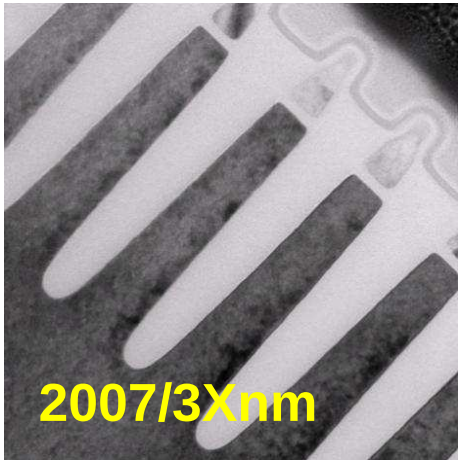

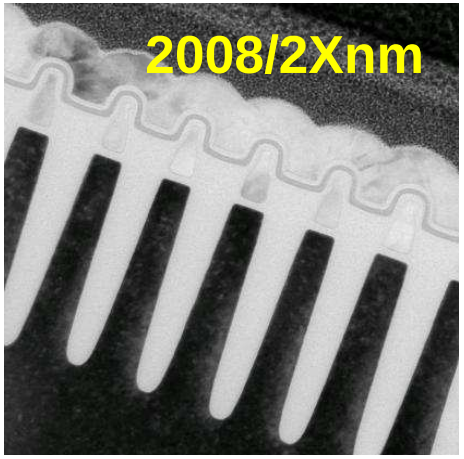

Bibliography

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