

COLLIDING PULSE PHASE DETECTOR FOR PICOSECOND RESOLUTION TIMING MEASUREMENT

Indexing terms: Detectors, Measurement, Semiconductor devices

A phase detector consisting of Schottky diode peak detector taps distributed along an integrated GaAs transmission line has been fabricated. Pulses counterpropagate on the line, forward biasing taps in the region of pulse overlap. The relative phase gain, determined from the captured overlap function, is 20 mV/ps.

As computing and communication data rates move into the gigabit range, accurate phase and timing measurements of the associated integrated circuits become of critical importance. Phase shifters must be calibrated to picosecond accuracy, and digital systems now require clock skew and jitter measurements below 10 pS. Current timing measurement techniques use oscillator based vernier circuits, ramp generator circuits or tapped delay line circuits for one shot phase capture.¹⁻³ Vernier circuits and ramp generator circuits have good resolution, but poor measurement rate or throughput due to the required wait time while the data are processed. Tapped delay line circuits have good throughput due to the distributed nature of the detector but poor resolution due to the present hybrid nature of their construction. We describe a colliding pulse phase detector (CPPD) consisting of a monolithic GaAs tapped delay line circuit with peak detector taps. The CPPD has the throughput advantages of the tapped delay line capture technique, with much finer resolution because it is integrated and uses a pulse conditioning technique^{4,5} to achieve short electrical transients. The CPPD has been fabricated and its operation verified by steady state testing. A response of better than 20 mV of output voltage swing on the detector hold capacitors has been achieved for 1 pS of trigger input phase shift. Response is currently limited by the input slew rates and the periodic filter formed by the diode taps, and not the intrinsic speed of the taps themselves. When combined with preamps and analogue-to-digital converters (ADCs) this circuit should be capable of high throughput, subpicosecond resolution phase detection in steady state or in single shot mode.

The CPPD circuit shown in Fig. 1 consists of 128 pS of coplanar waveguide delay line integrated on a semi-insulating

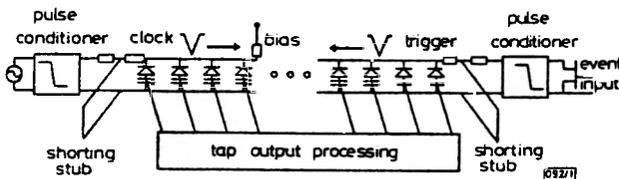


Fig. 1 Schematic diagram of colliding pulse phase detector

GaAs substrate with 16 Schottky diode peak detector taps spaced at 8 pS intervals along the line. A reference (clock) signal and an unknown event (trigger) signal are launched from opposite ends of the delay line. To realise a response from a peak detector based tapped delay line such as the CPPD the clock and trigger signals must both be short in duration as compared to the 128 pS delay time of the integrated delay line. Furthermore, circuit resolution is limited by the slew rates of the inputs. For these reasons pulse conditioning is used to improve the slew rates of the clock and trigger input signals. A 20 pS risetime step function is produced from both inputs by conditioning circuits. Final clock and trigger pulses of approximately 20 pS duration and 1 V and 500 mV in amplitude, respectively, are formed by differentiation using a shorted transmission line stub at the conditioner outputs. The two pulses are coupled into the coplanar waveguide as shown in Fig. 1, with the resistors forming termination for both the compressor driver and the delay line. To minimise the effect of dispersion due to the transmission line filter formed by the periodic structure of the tapped delay line, a

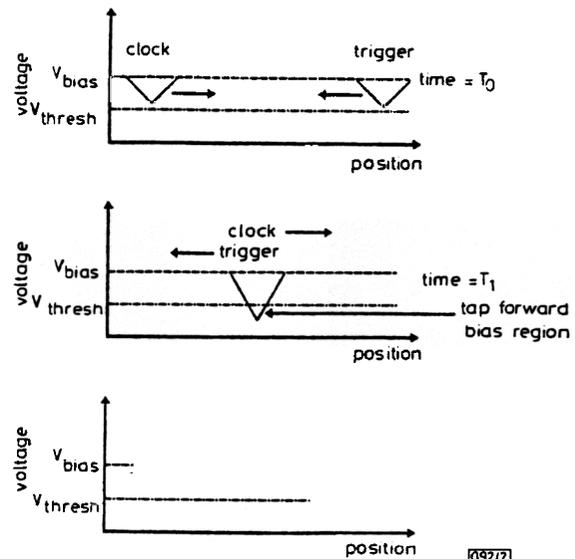


Fig. 2 Collision process shown schematically

At time T_0 two pulses are coupled onto delay line
Pulses overlap and exceed threshold of detector diodes at time T_1 in centre region of detector only
At time T_3 attenuated pulses are shown after collision travelling toward terminations at each end

single tap actually consists of four diodes distributed at 2 pS effective delay time along the line and tied together at the tap output.

Fig. 2 shows the evolution of the coincidence of two input pulses. The peak detector taps are biased such that neither the clock nor the trigger signal alone is large enough in amplitude to cause forward bias of the peak detector taps. This is the case at times T_0 and T_2 . At time T_1 , however, there is coincidence of the two pulses and forward bias occurs, capturing a convolution of the two pulses on the tap hold capacitors. After a collision event is captured the outputs of the taps must be analysed. Digitising the tap outputs with comparators or ADCs is the preferred method of phase recovery. The present setup, however, does not yet include this tap processing circuitry. Instead, the response of the CPPD was measured using a steady state mixing technique. The clock is driven at a harmonic of the trigger input plus an offset. The response is filtered and displayed on a low frequency oscilloscope at the offset frequency. The waveforms shown in Fig. 3 are the outputs of two adjacent taps, spaced 8 pS apart in delay time. The change in hold capacitor voltage is seen on the oscilloscope as the trigger pulse is swept through the clock pulse at the tap. In steady state operation the CPPD has a peak output response of 20 mV of output voltage change per picosecond of input phase shift. This is simply measured as the output signal slew rate achieved at each tap. The clock frequency used for the structure reported here was 7 GHz. The

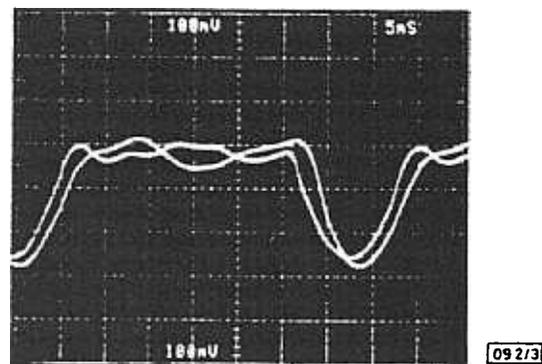


Fig. 3 Equivalent time output of two adjacent taps

8 pS delay difference between two taps is clearly resolvable
Vertical scale is 100 mV/division and actual time scale represented by equivalent time output is 19 ps/division

trigger circuit is designed to operate at frequencies from 50 MHz to over 1 GHz. It was operated at 1.4 GHz in this experiment. Further, no reverse bias was applied to the tap diodes, thereby allowing the delay line to selfbias. This allows all of the reflections due to discontinuities on the line to be seen at the tap outputs. This 'clutter' represents the principal error component of the detection scheme and must be minimised.

To predict one-shot response the loading effects of a prospective preamp must be examined. The GaAs Schottky diodes used for the taps have a zero bias capacitance of about 14 fF and a series resistance of about 12 Ω . The integrated hold capacitors are 100 fF. The charging time of the peak detector circuit is the effective resistance seen by the hold capacitor consisting of the dynamic and series resistance of the diode (about 25 Ω total) plus the output impedance of the 50 Ω transmission line in two directions (equaling 25 Ω) multiplied by the hold capacitor value. The time constant for charging the hold capacitor, then, is approximately 5 pS. Thus, pulses in the current circuit are about four time constants long, easily enough for significant charging of the hold capacitors. Finally, the loading effect of a GaAs preamp integrated on the same substrate as the CPPD should be no more than an additional 100 fF load. This is the approximate gate capacitance of a 40 μm D-MESFET which could be used to buffer the hold capacitor signal. The preamp itself might be used as the hold capacitor except that the required proximity of the FET to the delay line would make circuit layout difficult. After further power gain the tap signal could then be sent off-chip to the tap processing circuit. The expected response in single shot mode then is reduced by about a factor of two from the steady state measurements due to the loading of a preamp, which has an input capacitance about equal to that of the hold capacitor. This implies a response of 10 mV/ps in single shot mode, still an easily detectable signal.

In conclusion, an integrated tapped delay line structure consisting of a coplanar waveguide transmission line with Schottky diode peak detector taps has been fabricated. The structure was driven with two pulse compressor circuits

producing two 20 pS pulse trains. The relative phases of the two inputs were determined from the position along the structure of the collision event as captured by the hold capacitors. Shifts of 1 pS in the trigger input signal were easily detectable during steady state testing of the structure. Improvements in the current resolution should be possible with better pulse compression circuits yielding greater slew rates for input pulses and reduced dispersion due to tap discontinuities by further distribution of the taps along the line. Finally, when coupled with external processing circuitry the CPPD should be capable of picosecond resolution detection of trigger events in one-shot or in steady state.

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